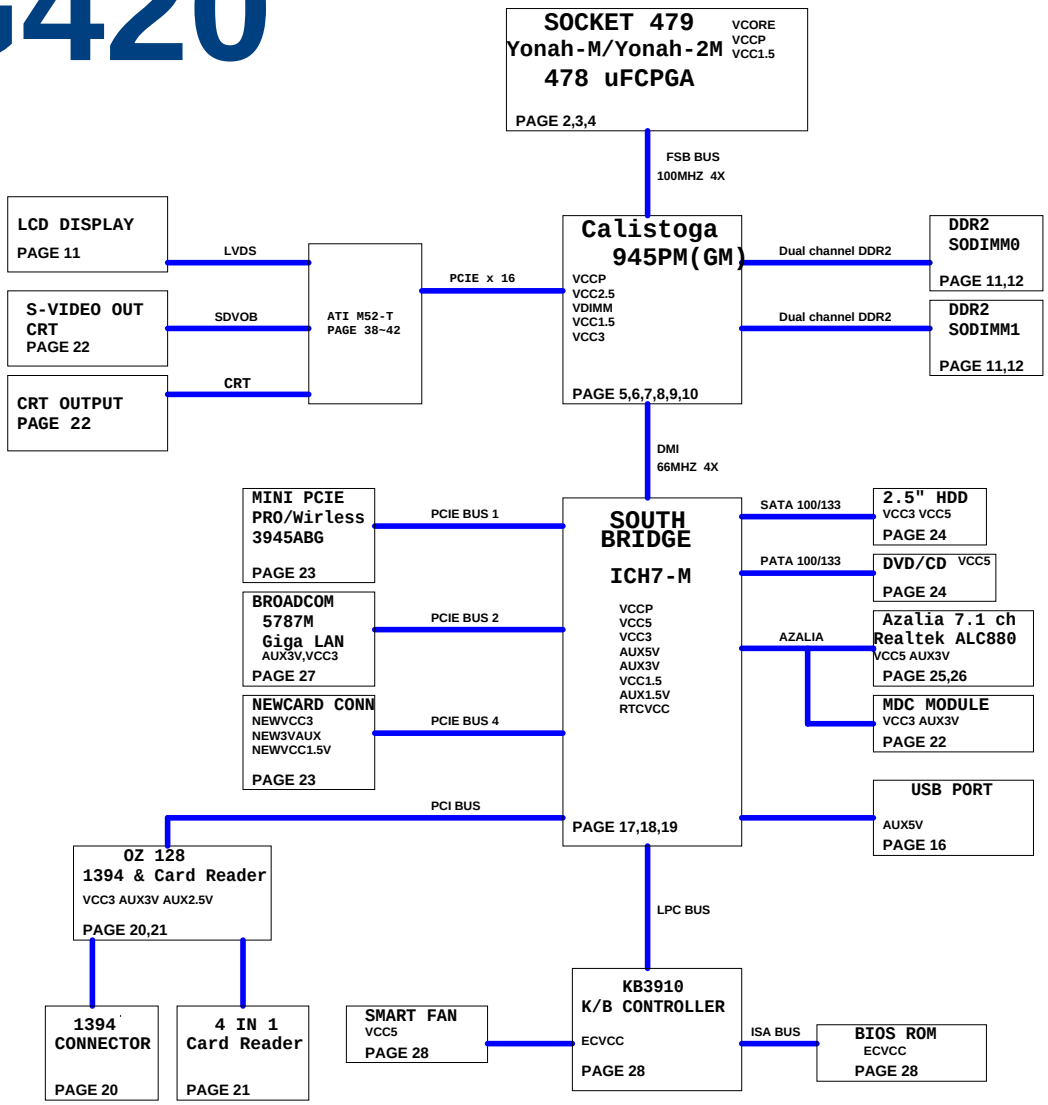
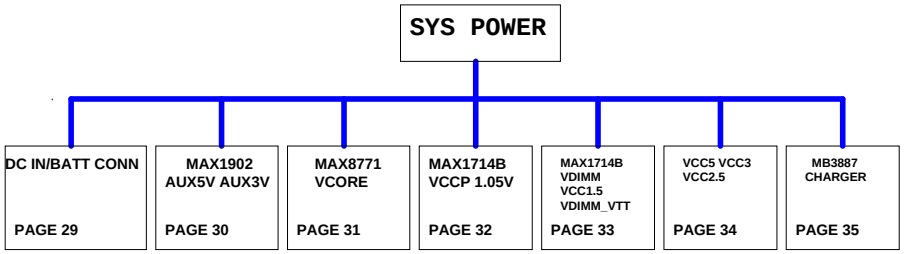
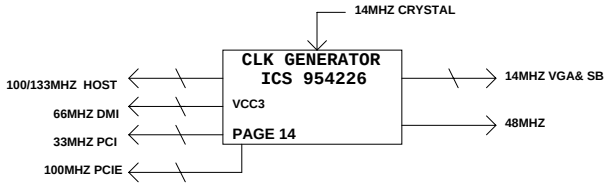
G420





RTC AND POWER CONTROL
PAGE 17



POWER SEQUENCE BLOCK DIAGRAM
PAGE 36

HISTORY
PAGE 37

PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
REV	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0
DATE	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03

PAGE	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36
REV	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0
DATE	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03

PAGE	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54
REV	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0										
DATE	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03										

PCB P/N:15-F73-013000

Approved by	Checked by	Designed by

P.Leader
Simon

Elitegroup Computer Systems

Title: G420 BLOCK DIAGRAM

Size: A2 | Document Number: 420 -1-4-01 | Rev: 3.0

Date: Monday, August 21, 2006 | Sheet 1 of 44

Place testpoint on
IERR- with GND
0.1" away

VCCP

IERR- R83 1 2 56_0402
HTMS SR52 1 2 54.9_1%_0402
HTDI SR53 1 2 54.9_1%_0402
CPU_PWRGD SR83 200_0402

HTCK SR49 1 2 54.9_1%_0402
HTRST- R61 1 2 680_0402

VCCP 0.5" max length
SR50 1K_1%_0402
GTLREF
SR46 2K_1%_0402
CLOSE TO CPU

SU2A

ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERM
H CLK
RESERVED

Yonah Ball-out Rev 1.0

SU2B

DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC

Yonah Ball-out Rev 1.0

Hcomp 0~3 0.5" max length
Close to CPU

R112 51 ohm:
Intel has determined that Test2 pin needs to be populated with a 51 ohm +/-5% resistor in order for Yonah B-0 silicon to boot due to issue in the reset sequence needed for the processor.

Remote and Local Thermal Sensor

SU3
MAX6648_MSOP-8

THERM ALERT

BAS316_SOD323_NC

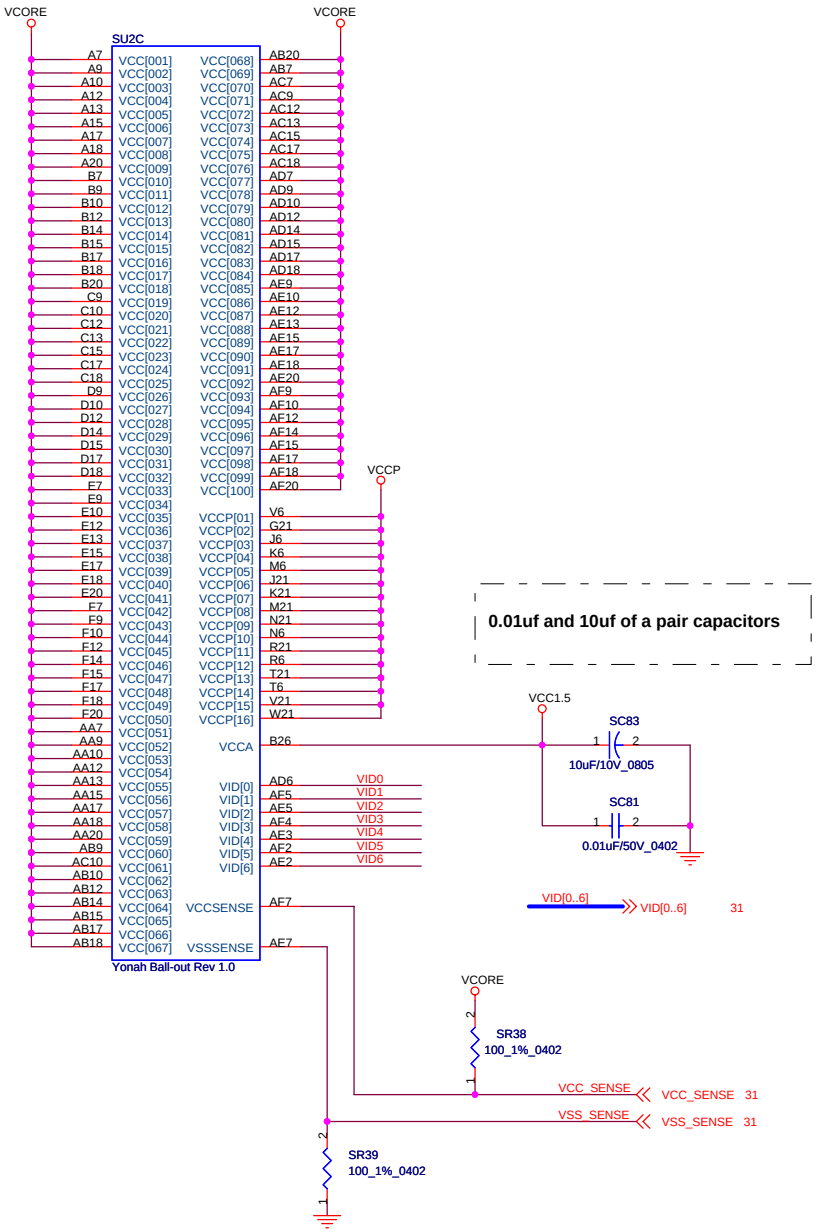
BSEL[0]	BSEL[1]	BSEL[2]	BCLK frequency
L	L	L	RESERVED
H	L	L	133MHZ
L	H	L	RESERVED
H	H	L	166MHZ

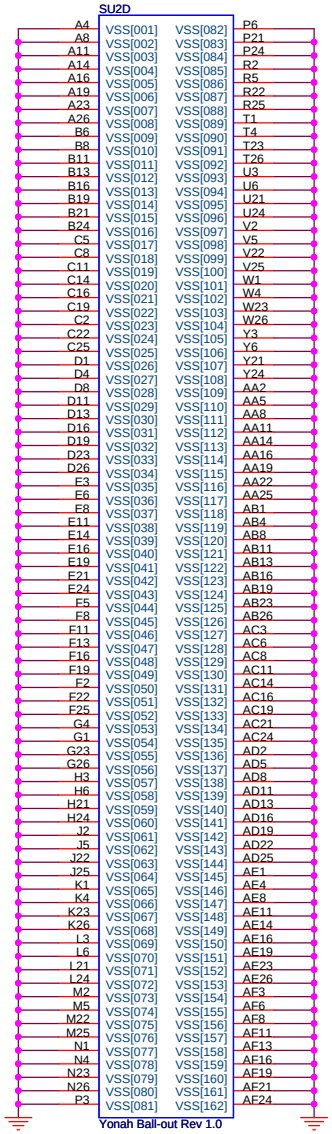
Elitegroup Computer Systems

Title: G420 Yonah-1

Size: A3 | Document Number: 420 -1-4-01 | Rev: 3.0

Date: Thursday, August 03, 2006 | Sheet 2 of 44





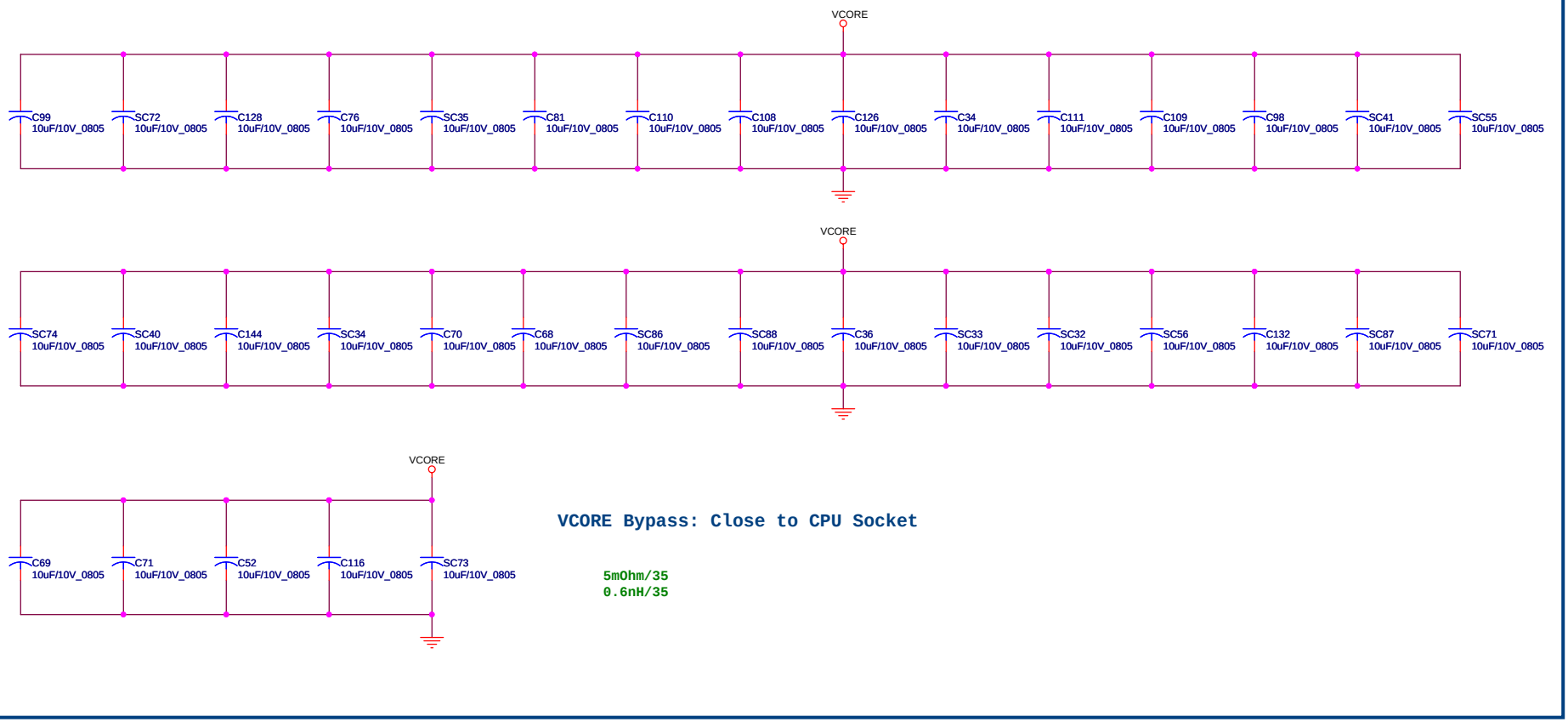
Layout Note:
Route VCC_SENSE and VSS_SENSE trace at 27.4 ohm with 50 mil spacing.
Place PU and PD within 1 inch of CPU.

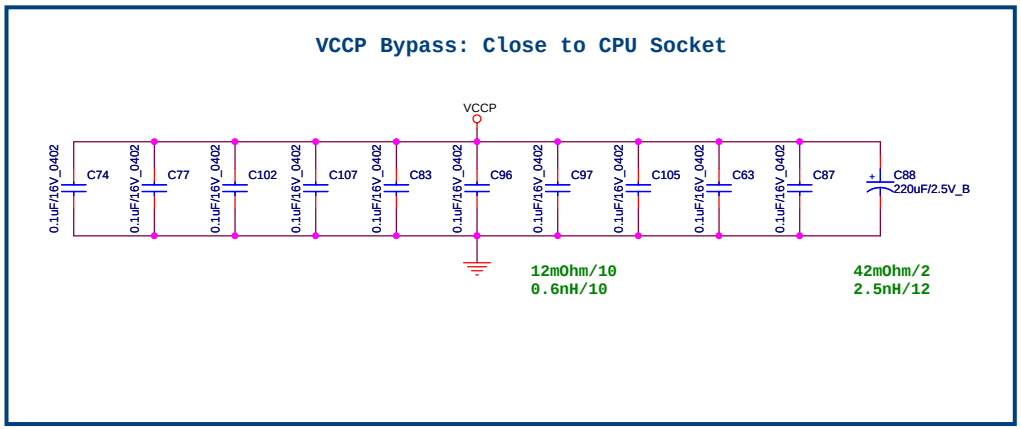
Elitegroup Computer Systems

Title: **G420 Yonah-2**

Size	Document Number	Rev
A3	420 -1-4-01	3.0

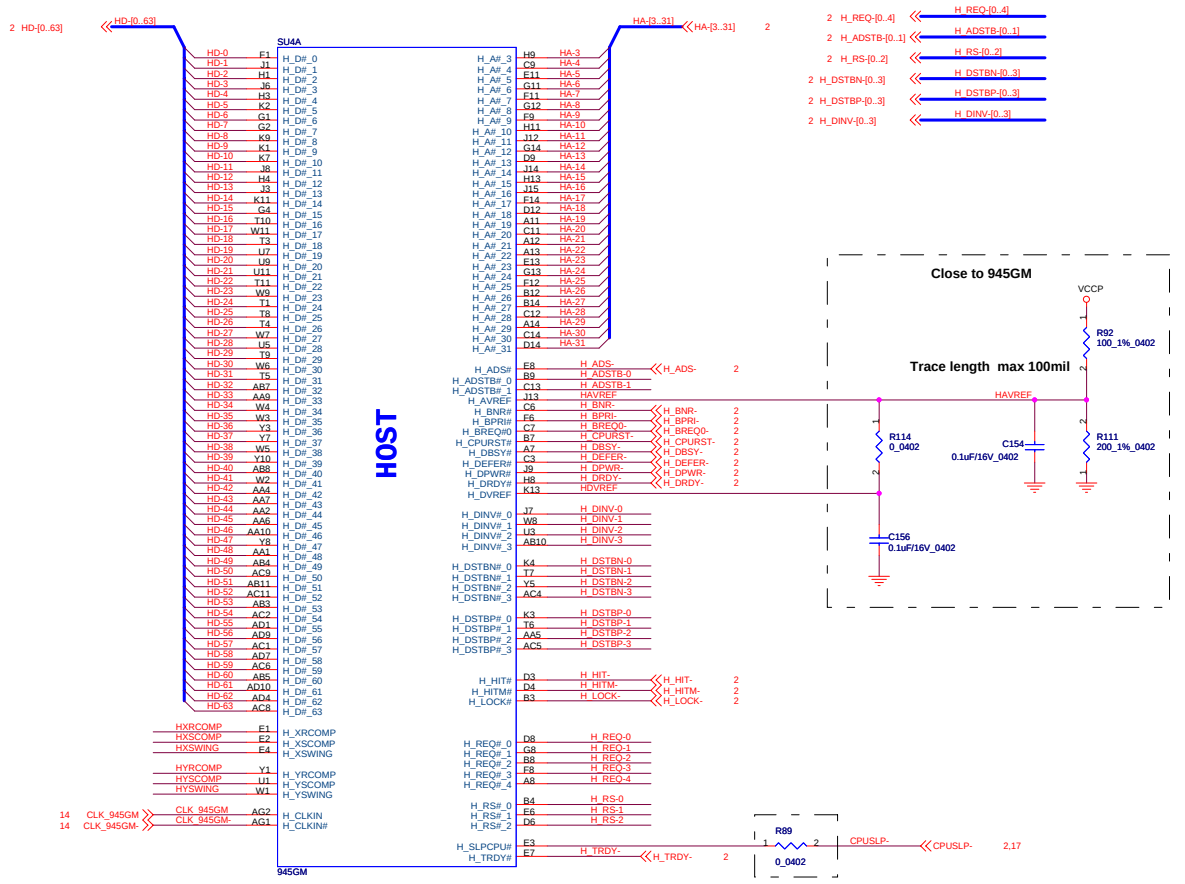
Date: Thursday, August 03, 2006 Sheet 3 of 44



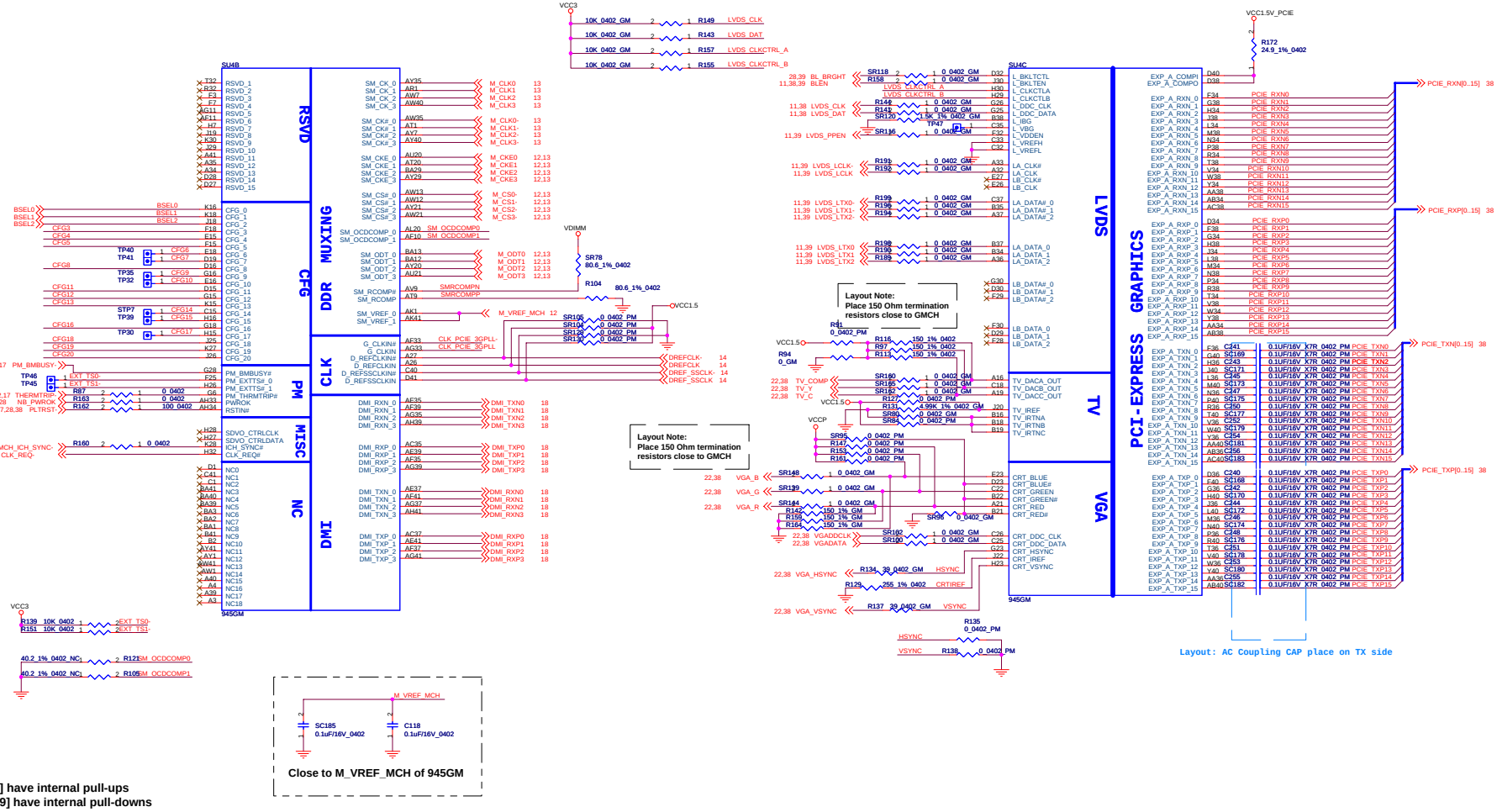


Elitegroup Computer Systems

Title: G420 Yonah-3		
Size: B	Document Number: 420 -1-4-01	Rev: 3.0
Date: Thursday, August 03, 2006	Sheet 4 of 44	



Company	Elitegroup Computer Systems
Title	G420 945PM(GM)_A (HOST)
Size	C
Document Number	420 -1-4-01
Rev	3.0
Date:	Thursday, August 03, 2006
Sheet	5 of 44



CFG[3:17] have internal pull-ups
CFG[18:19] have internal pull-downs

CFG[2:0]
001= FSB 533 MHZ
011= FSB 667 MHZ

CFG[4:3]
00 = DDR 800
01 = DDR 533(default)
10 = DDR 667
11 = DDR 400

CFG5
LOW=DMIx2
HIGH=DMIx4 (default)

CFG6
LOW=Reserved
(DDR2 for MOBYDICK)
HIGH=DDR2

CFG7 (CPU Strap)
LOW=RSVD
HIGH=Mobile CPU (default)

CFG8 (LP PCIe)
LOW=Normal Mode
HIGH=Low Power Mode

CFG9(PCIE Graphics Lane)
LOW= Reversal Lane
HIGH=Normal Operation (default)

CFG10 (HOST PLL VCC SELET)
LOW=Reserved
HIGH=MOBILITY

CFG11 (PSB 4X CLK ENABLE)
LOW= 4X ENABLED
HIGH=8X ENABLED

CFG[13:12]
00=Partial Clock Gating Disable
01=XOR Mode Enable
10=All-Z Mode Enable
11=Normal Operation (Default)

CFG14 DF STRAP ENABLE
LOW=DF STRAP ENABLE
HIGH=Normal Operation

CFG15 (ICH RESET DISABLE)
LOW= ICH RESET DISABLE
HIGH=Normal Operation

CFG16 (FSB Dynamic ODT)
LOW=Dynamic ODT Disabled
HIGH=Dynamic ODT Enabled (default)

CFG17(Global Rcomp Disable)
LOW=All Rcomp Disable
HIGH=Normal Operation

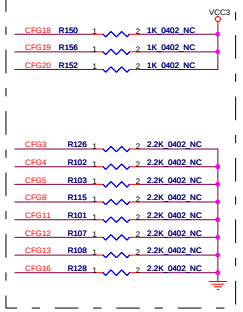
CFG18 (VCC SELECT)
LOW=1.05V (default)
HIGH=1.5V

CFG19 (DMI LANE RESERVED)
LOW=Normal
HIGH=LANES REVERSED (default)

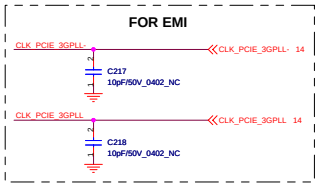
CFG20 (PCIe Backward Interpoerbility mode)
LOW=only SDVO or PCIE x1 is operational (defaults)

HIGH=SDVO and PCIE x1 are operating simultaneously via the PEG port

945GM CFG strapping



FOR EMI

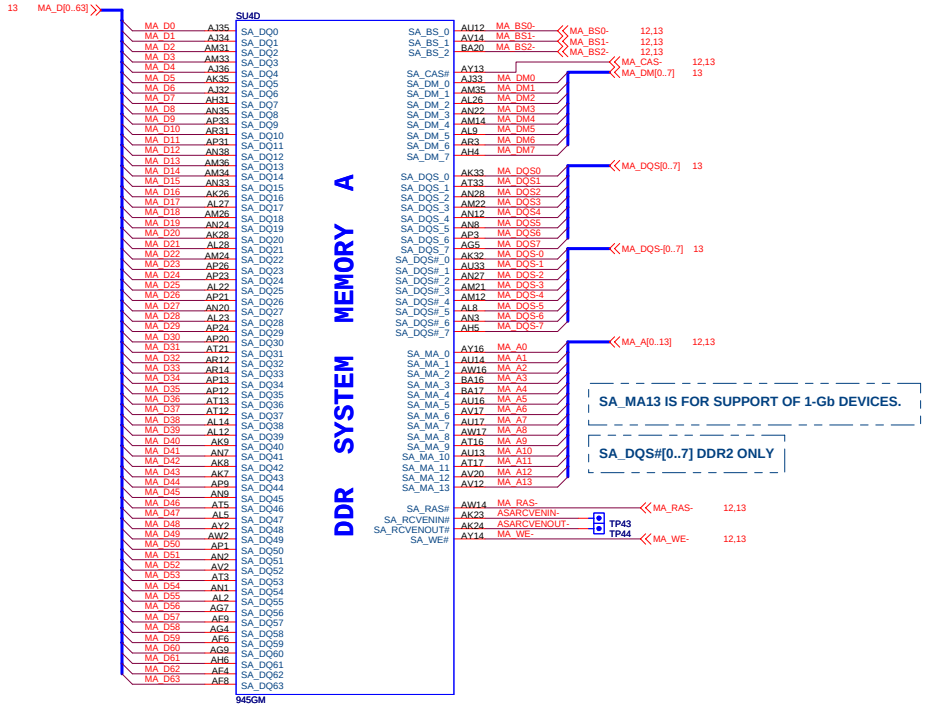


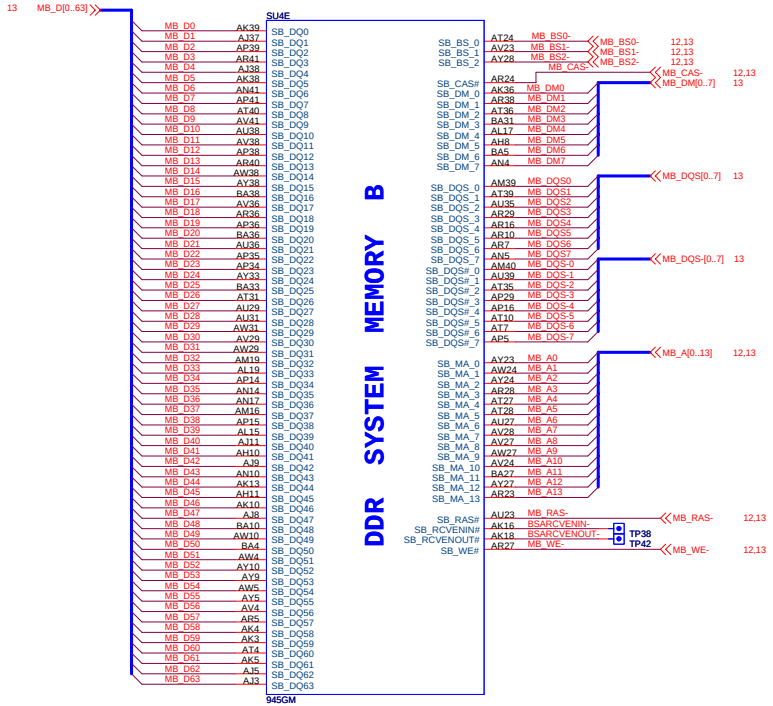
Elitegroup Computer Systems

Title: G420 945PM(GM)_B (VGA,DMI)

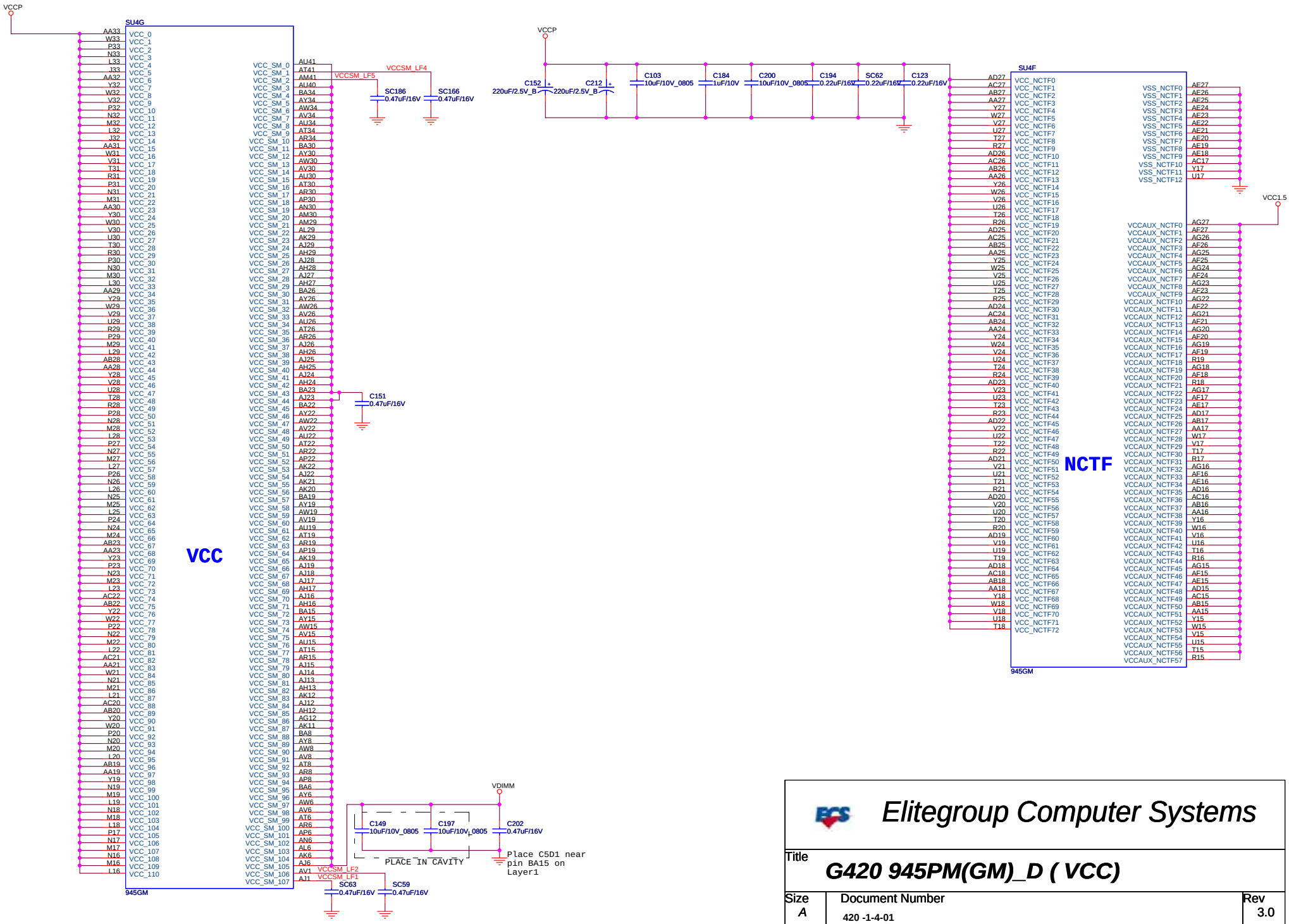
Size: Custom | Document Number: G420 -1-4-01 | Rev: 3.0

Date: Thursday, August 03, 2006 | Sheet 6 of 44





Elitegroup Computer Systems		
Title: G420 945PM(GM)_C (DDR)		
Size: C	Document Number: 420 -1-4-01	Rev: 3.0
Date: Thursday, August 03, 2006	Sheet 7 of 44	

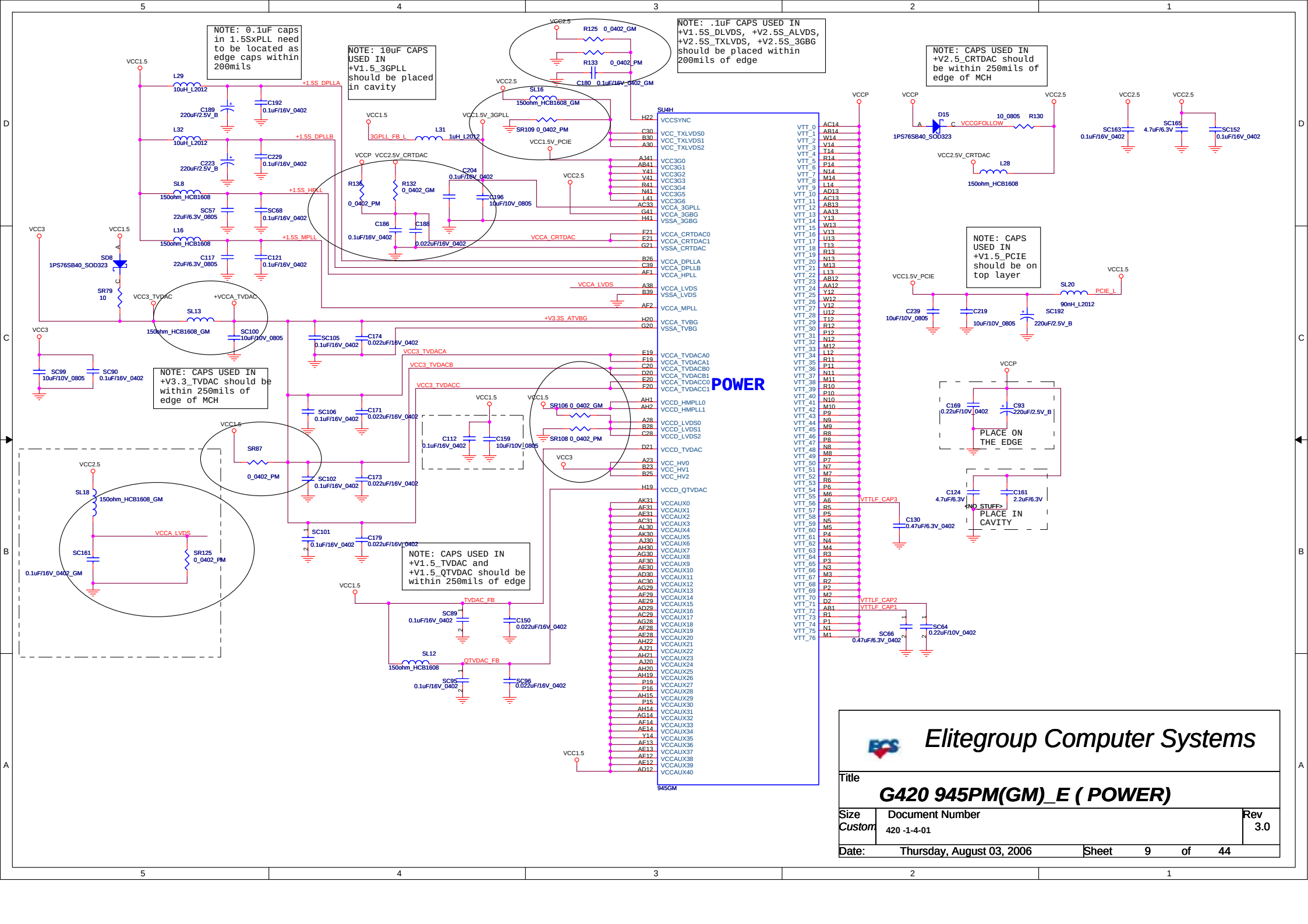


Elitegroup Computer Systems

Title: G420 945PM(GM)_D (VCC)

Size	Document Number	Rev
A	420 -1-4-01	3.0

Date: Thursday, August 03, 2006 Sheet 8 of 44


NOTE: 0.1uF caps in 1.5SxPLL need to be located as edge caps within 200mils
NOTE: 10uF CAPS USED IN +V1.5_3GPLL should be placed in cavity
NOTE: .1uF CAPS USED IN +V1.5S_DLVDS, +V2.5S_ALVDS, +V2.5S_TXLVDS, +V2.5S_3GBG should be placed within 200mils of edge
NOTE: CAPS USED IN +V2.5_CRTDAC should be within 250mils of edge of MCH
NOTE: CAPS USED IN +V1.5_PCIE should be on top layer
NOTE: CAPS USED IN +V3.3_TVDAC should be within 250mils of edge of MCH
NOTE: CAPS USED IN +V1.5_TVDAC and +V1.5_QTVDAC should be within 250mils of edge
PLACE ON THE EDGE
PLACE IN CAVITY
POWER
SU4H
945GM
Elitegroup Computer Systems
Title
G420 945PM(GM)_E (POWER)
Size Custom
Document Number 420 -1-4-01
Rev 3.0
Date: Thursday, August 03, 2006
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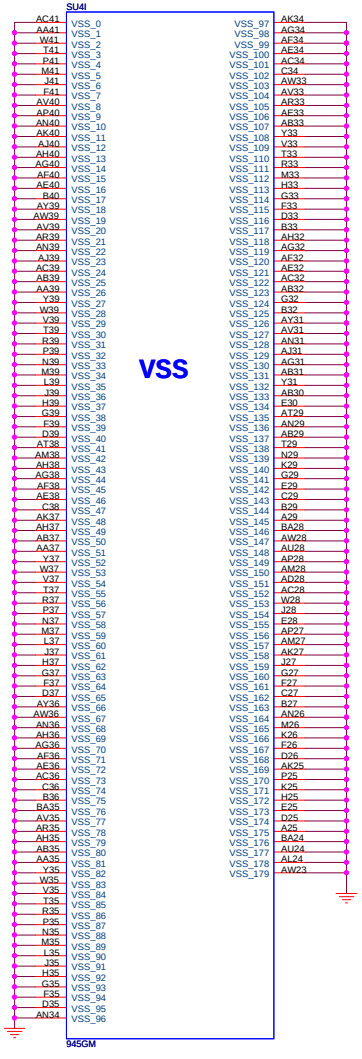
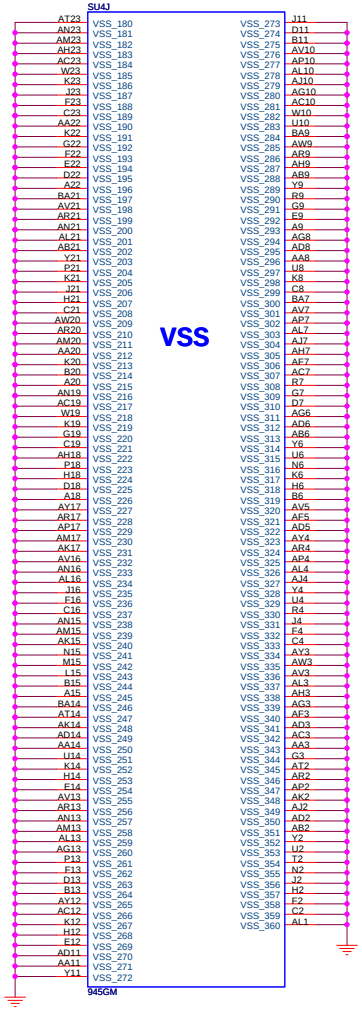
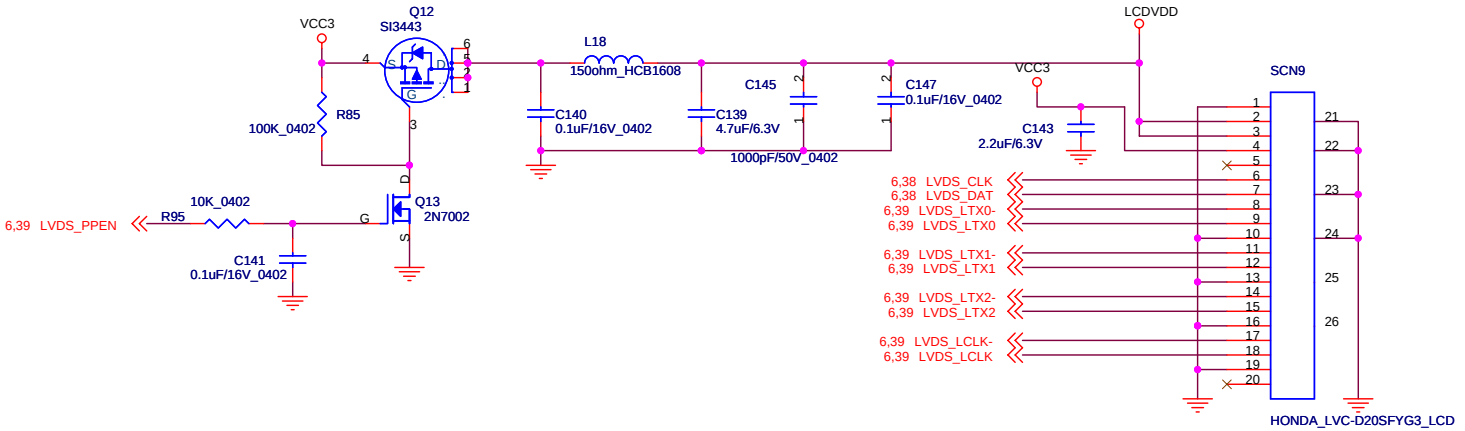
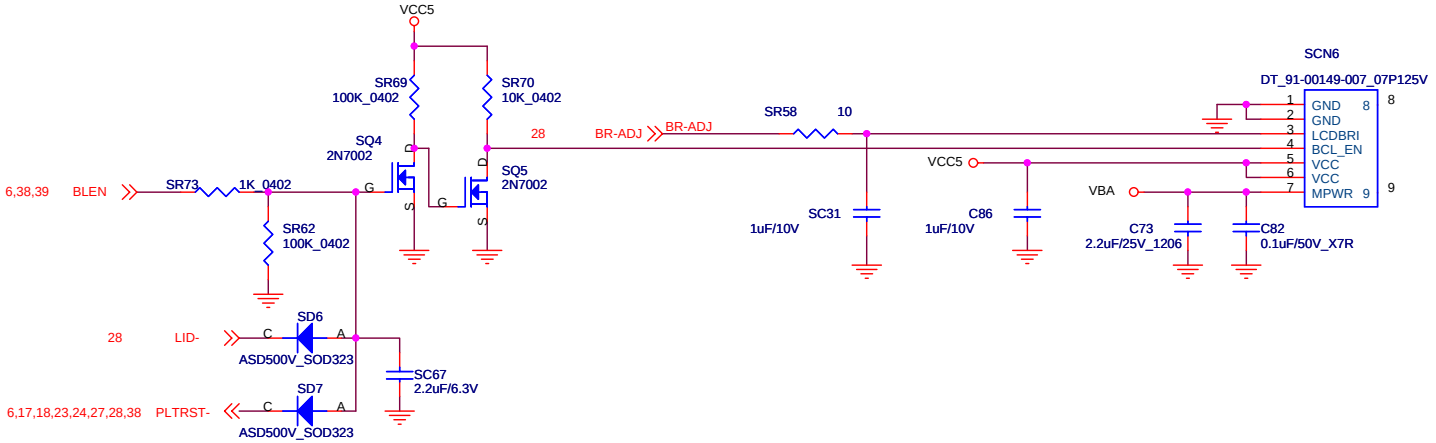


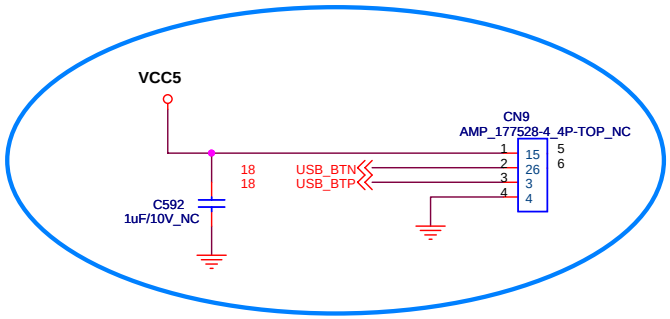


Elitegroup Computer Systems

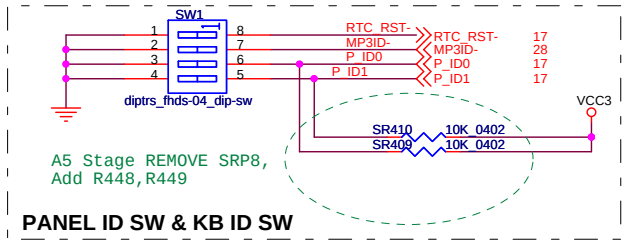
Title	G420 945PM(GM)_F (VSS)	
Size: C	Document Number: 420 -1-4-01	Rev: 3.0
Date: Thursday, August 03, 2006	Sheet 10 of 44	







V1.0 Stage BOM Del CN9,C592

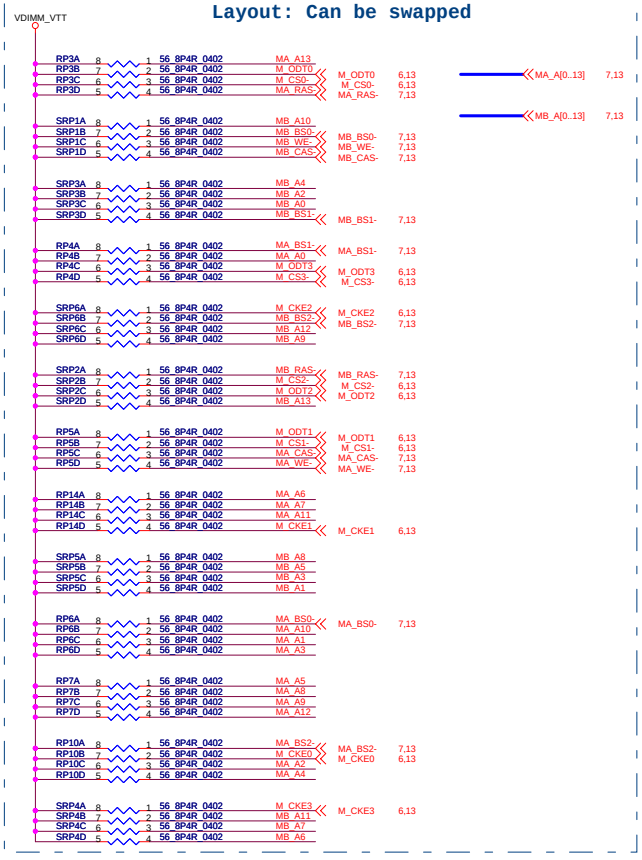


PANEL ID SW & KB ID SW

Elitegroup Computer Systems

Title: G420 LVDS		
Size: Custom	Document Number: 420 -1-4-01	Rev: 3.0
Date: Thursday, August 03, 2006	Sheet 11 of 44	

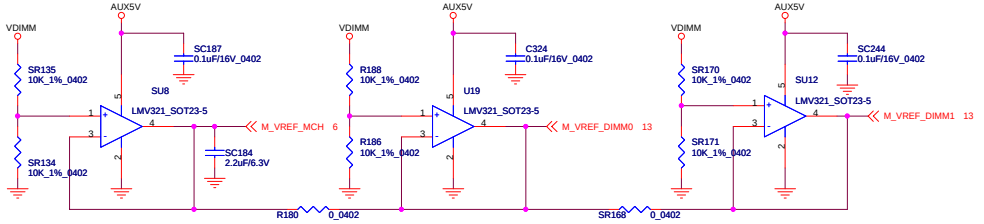
Layout: Can be swapped



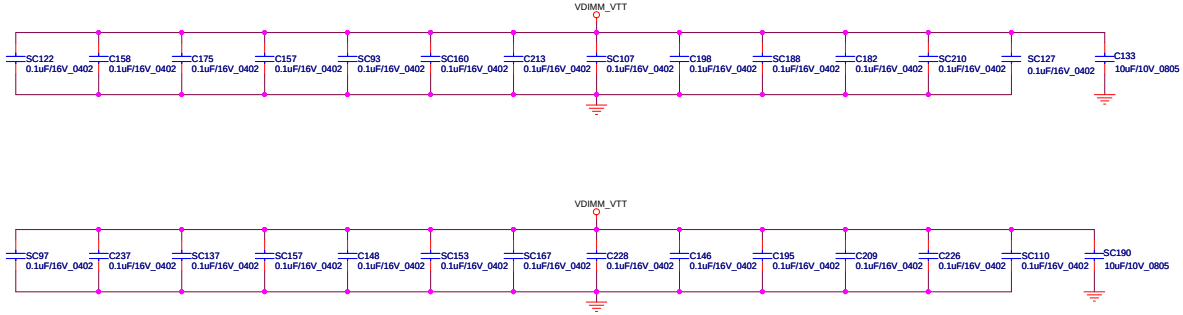
Close to MCH
R90 R95 CLOSE TO MCH
U6 CLOSE TO M_VREF_MCH

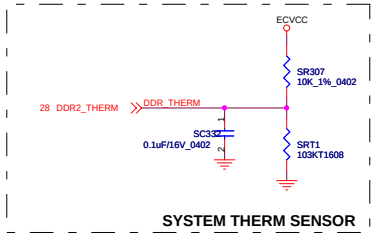
Close to DIMM0
R91 R93 CLOSE TO DIMM0
U4 CLOSE TO M_VREF_DIMM0

Close to DIMM1
R92 R94 CLOSE TO DIMM1
U5 CLOSE TO M_VREF_DIMM1



Every 2 Resistors with 1 CAP





Elitegroup Computer Systems

Title: G420 DDR2 VTT

Size: C | Document Number: 420 -1-4-01 | Rev: 3.0

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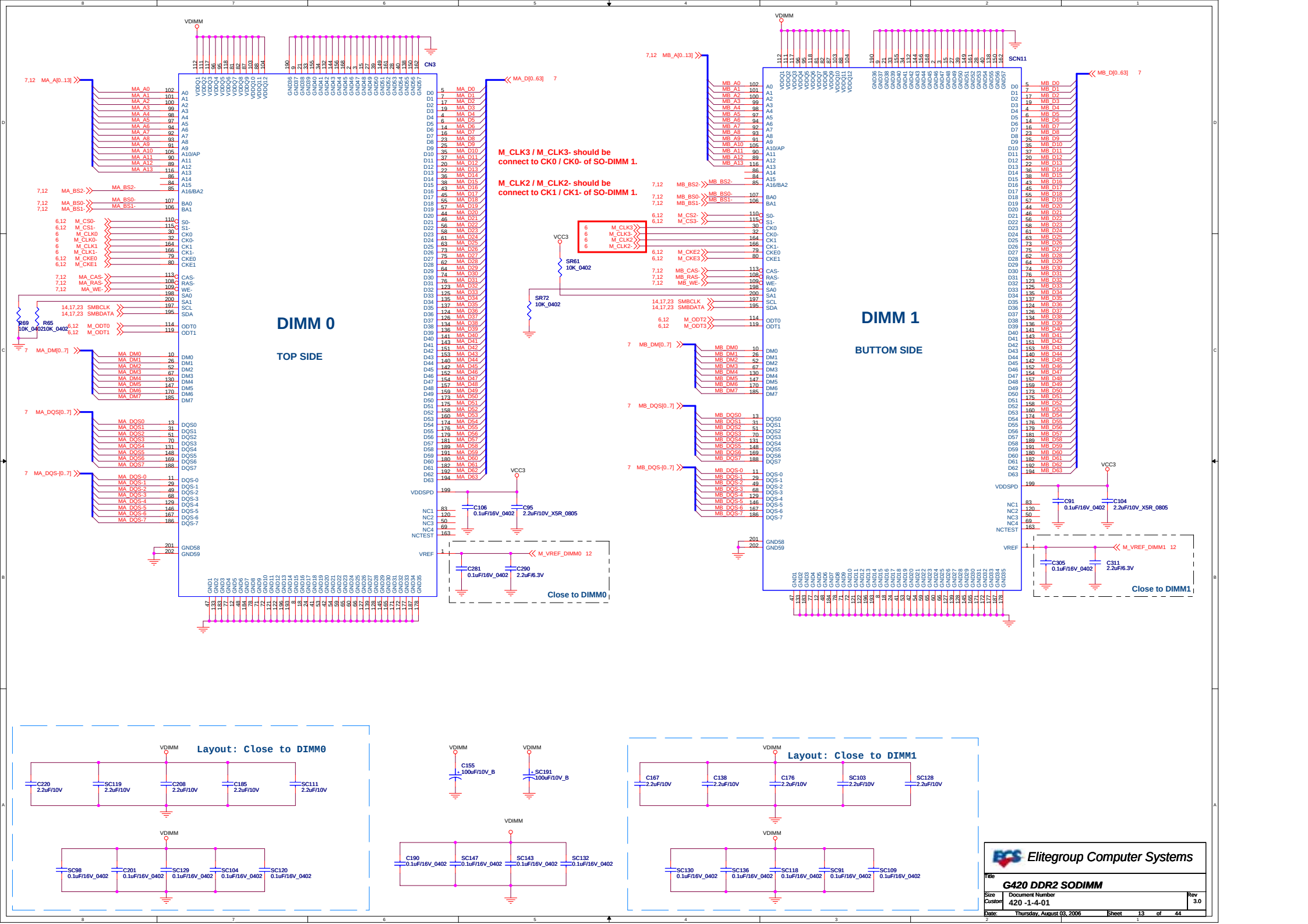
DIMM 0
TOP SIDE
DIMM 1
BUTTOM SIDE
CN3
SCN11
M_CLK3 / M_CLK3- should be connect to CK0 / CK0- of SO-DIMM 1.
M_CLK2 / M_CLK2- should be connect to CK1 / CK1- of SO-DIMM 1.
SR61 10K_0402
SR72 10K_0402
R69 10K_0402
R65 10K_0402
Close to DIMM0
Close to DIMM1
Layout: Close to DIMM0
Layout: Close to DIMM1
C220 2.2uF/10V
SC119 2.2uF/10V
C208 2.2uF/10V
C185 2.2uF/10V
SC111 2.2uF/10V
SC98 0.1uF/16V_0402
C201 0.1uF/16V_0402
SC129 0.1uF/16V_0402
SC104 0.1uF/16V_0402
SC120 0.1uF/16V_0402
C155 100uF/10V_B
SC191 100uF/10V_B
C190 0.1uF/16V_0402
SC147 0.1uF/16V_0402
SC143 0.1uF/16V_0402
SC132 0.1uF/16V_0402
C167 2.2uF/10V
C138 2.2uF/10V
C176 2.2uF/10V
SC103 2.2uF/10V
SC128 2.2uF/10V
SC130 0.1uF/16V_0402
SC136 0.1uF/16V_0402
SC118 0.1uF/16V_0402
SC91 0.1uF/16V_0402
SC109 0.1uF/16V_0402
Elitegroup Computer Systems
G420 DDR2 SODIMM
Size Custom
Document Number 420 -1-4-01
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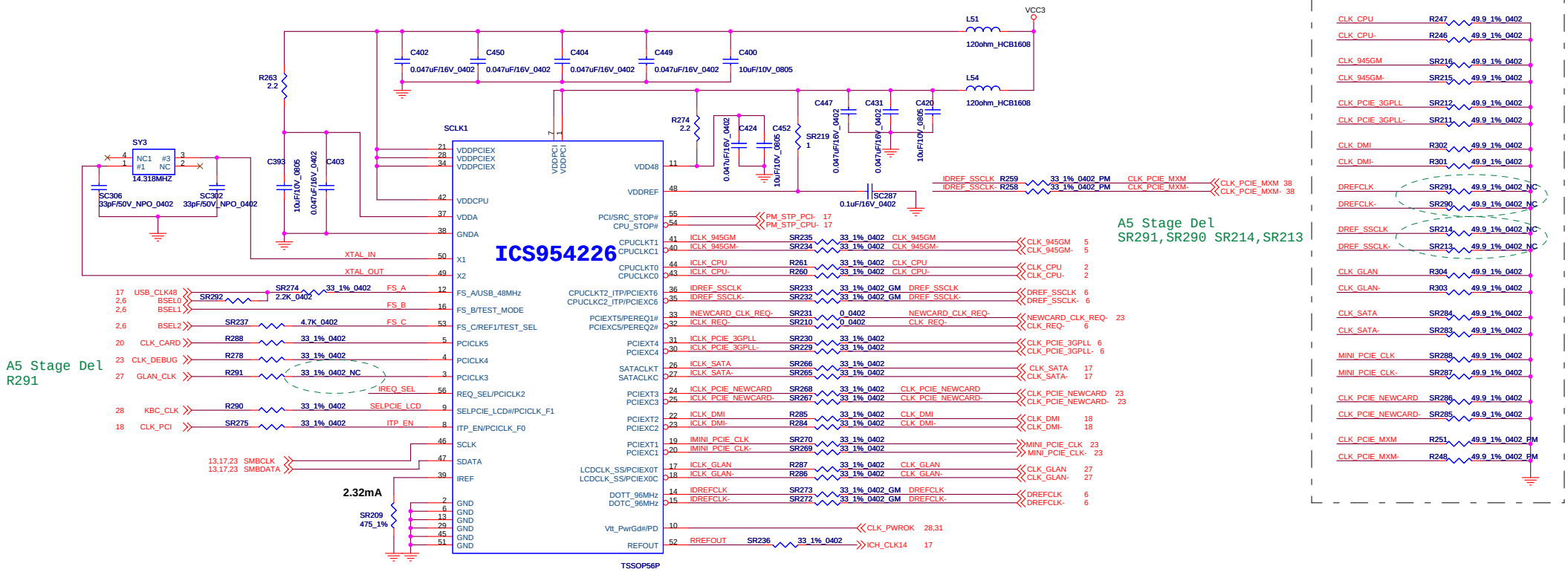
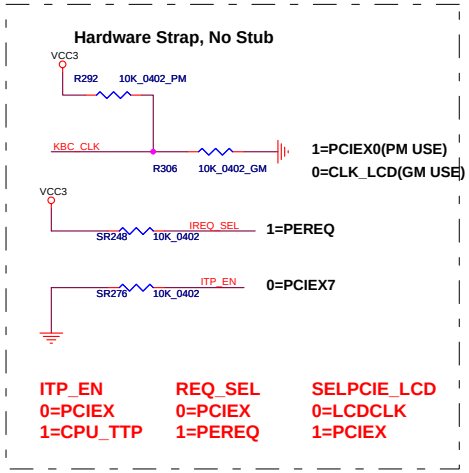
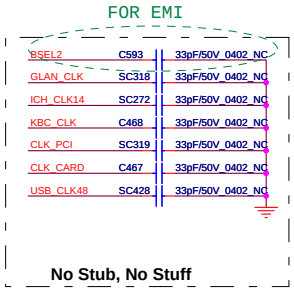
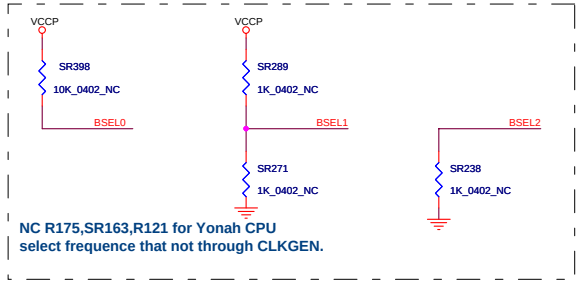
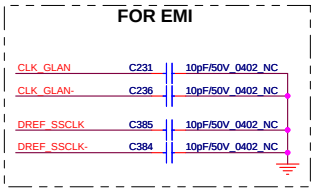










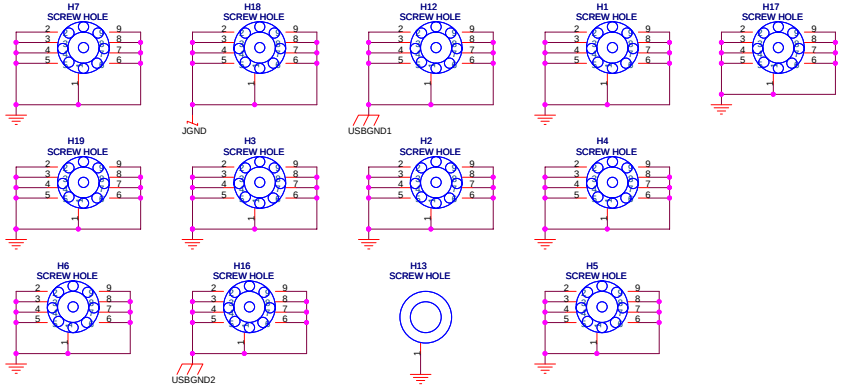
FS_A	FS_B	FS_C	CPU MHz	
BSEL0	BSEL1	BSEL2		FSB
1	0	1	100.00	400.00
1	0	0	133.33	533.00
1	1	1	200.00	
1	1	0	166.66	667.00
0	0	1	333.33	
0	0	0	266.66	
0	1	1	400.00	
0	1	0	200.00	

Elitegroup Computer Systems

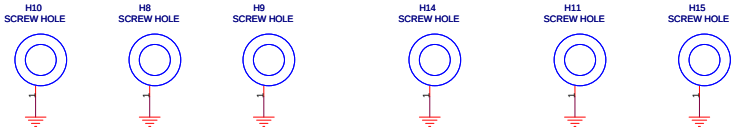
Title: G420 CLOCK GENERATOR

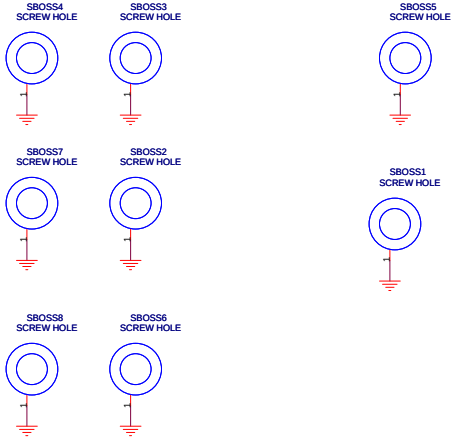
Size: Custom | Document Number: 420 -1-4-01 | Rev: 3.0

Date: Thursday, August 03, 2006 | Sheet 14 of 44



SYSTEM SCREW HOLE





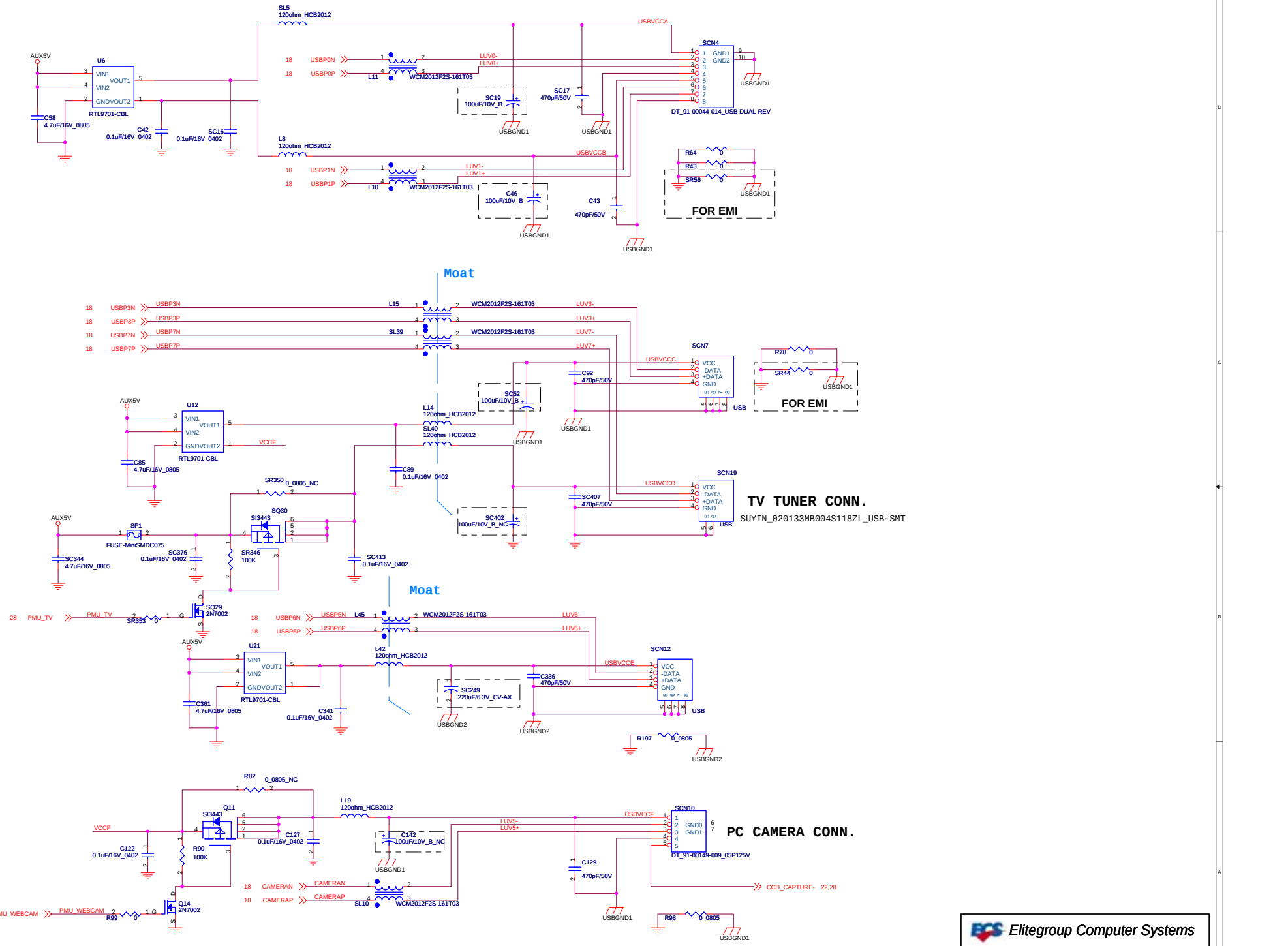
BOSS SCREW

Elitegroup Computer Systems

Title: **G420 SCREW HOLE**

Size	Document Number	Rev
C	420 -1-4-01	3.0

Date: Thursday, August 03, 2006 Sheet 15 of 44



Elitegroup Computer Systems		
Title: G420 USB PORT		
Size: Custom	Document Number: 420 -1-4-01	Rev: 3.0
Date: Thursday, August 03, 2006	Sheet 16 of 44	

ICH7 internal VR enable strap

I NTVRMEN	R426	R492
Enable (default)	1	STUFF	UNSTUFF
Disable	0	UNSTUFF	STUFF

RTC CIRCUIT

AS CLOSE AS TO ICH7

SR182 NC for Intel checklist recommand.

Placed Close to ICH7

Placed Close to ICH7

Close to ICH7

KBSCI-,KBSMI- from GPIO27,28 change to GPIO13,14.
KBSCI-,KBSMI- should be connect to SB GPIO[0:15]

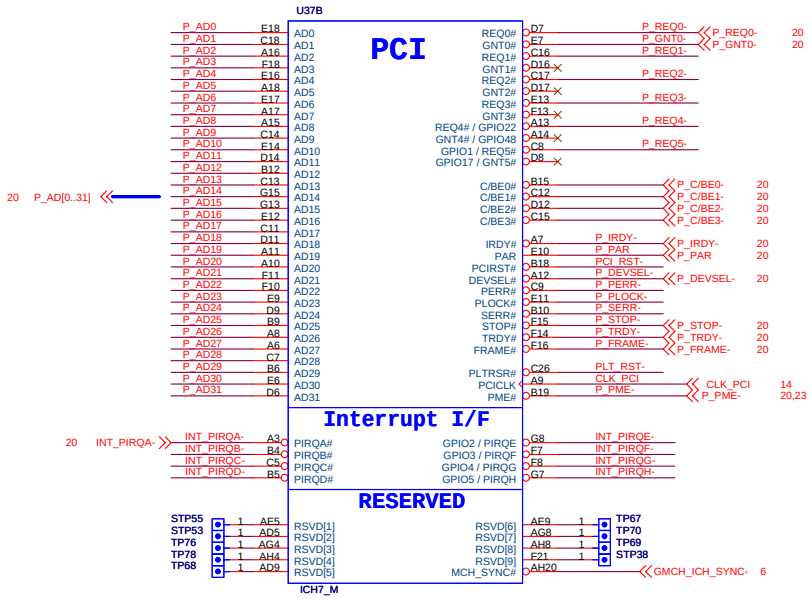
V1.0 Stage Add

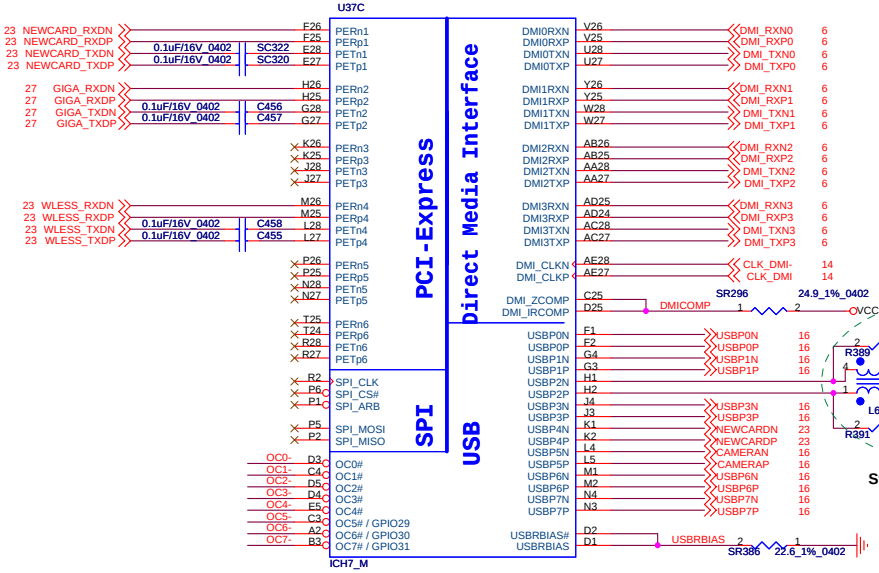
Elitegroup Computer Systems

Title: G420 ICH7-M(CPU/RTC/IDE/ACZ)

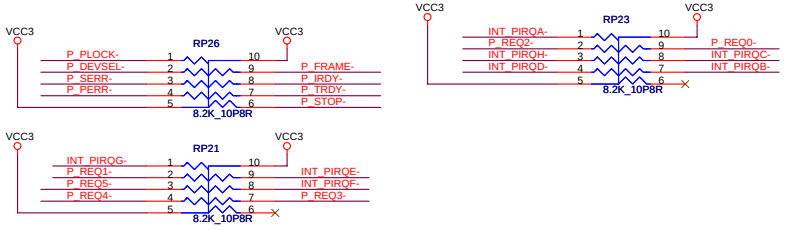
Size: Custom | Document Number: 420 -1-4-01 | Rev: 3.0

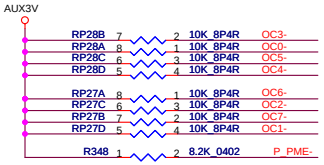
Date: Thursday, August 03, 2006 | Sheet 17 of 44

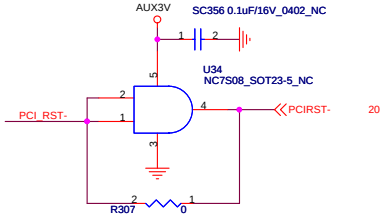


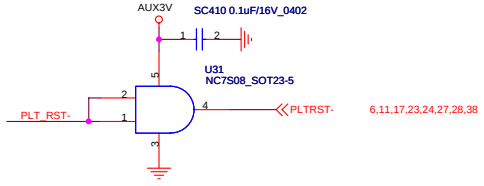


USBP0N USBP0P USBP1N USBP1P	CN5 (DUAL CONNECT)	USB4N USB4P	NEW CARD
		USB5N USB5P	CAMERA
USB2N USB2P	Blue Tooth Wireless (Option)	USB6N USB6P	CN8
USB3N USB3P	CN6	USB7N USB7P	CN7







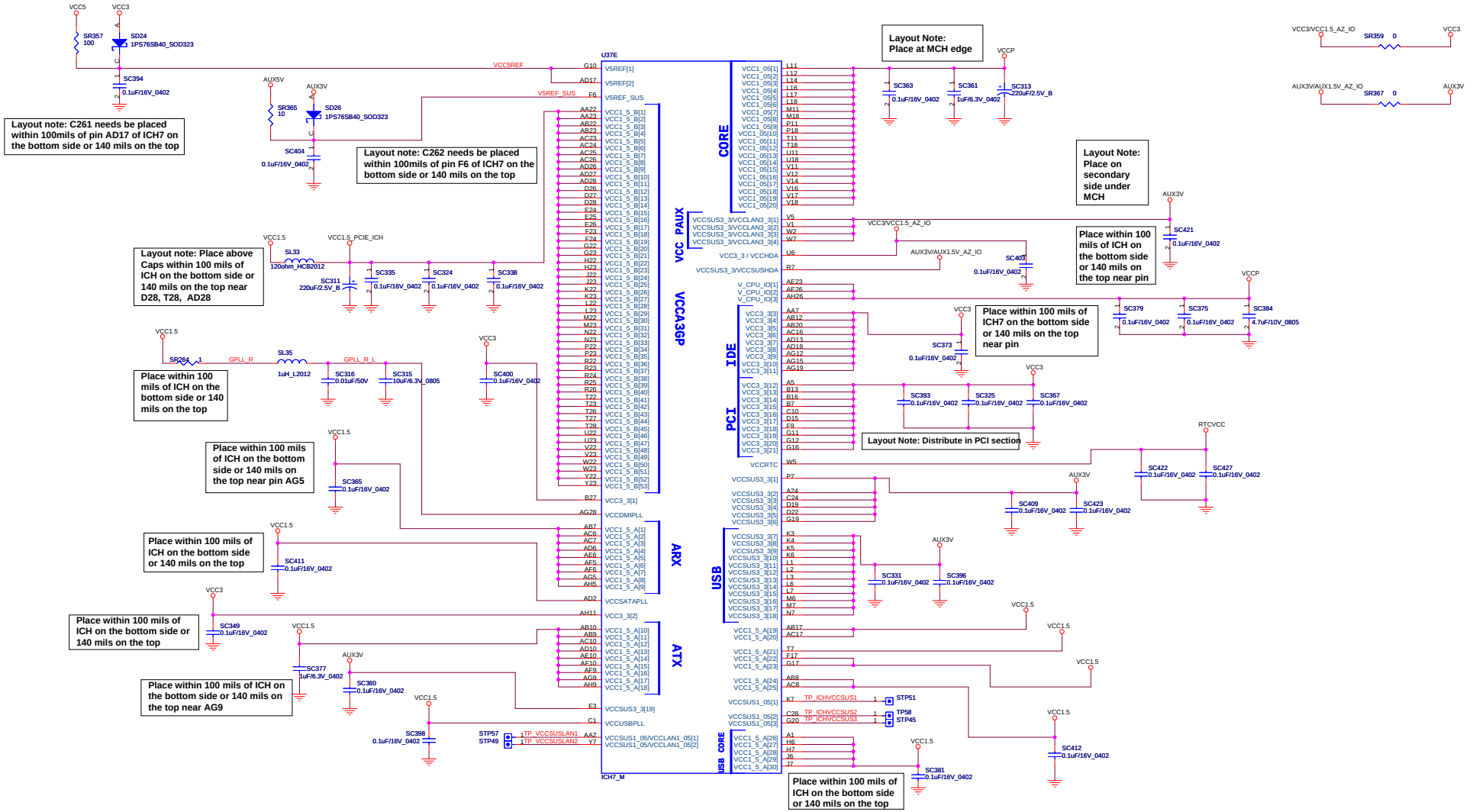


Elitegroup Computer Systems

Title: G420 ICH7-M(DMI/PCI/USB/PCIE)

Size	Document Number	Rev
Custom	420 -1-4-01	3.0

Date: Thursday, August 03, 2006 Sheet 18 of 44



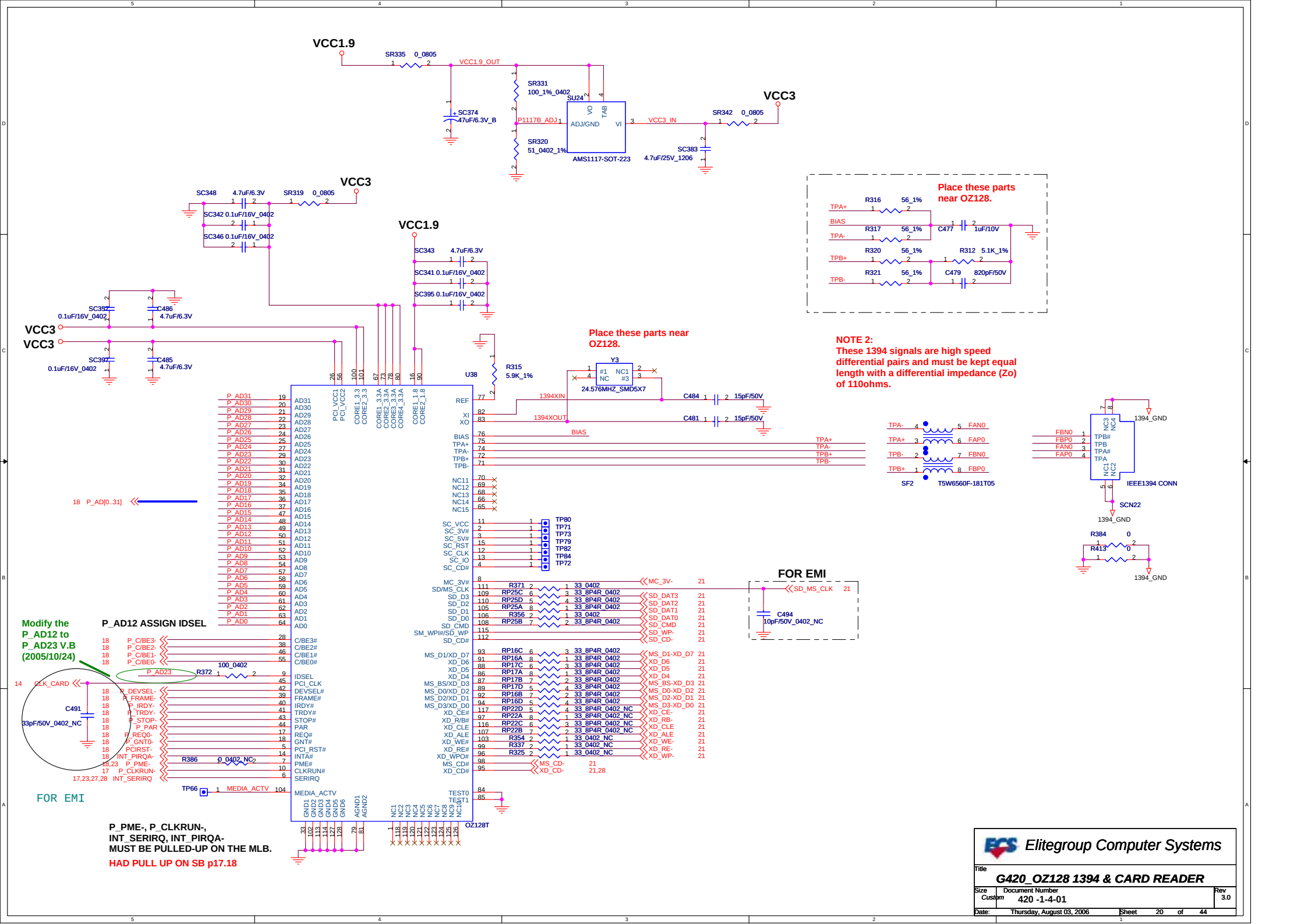
Elitegroup Computer Systems

Title

G420 ICH7-M(POWER & GND)

Size	Document Number	Rev
Custom	420 -1-4-01	3.0

Date: Thursday, August 03, 2006 Sheet 19 of 44

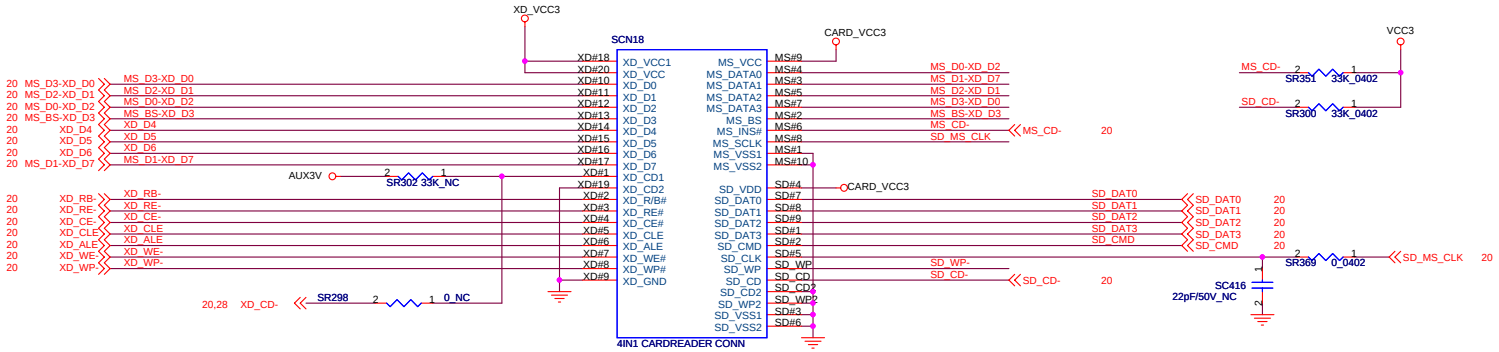


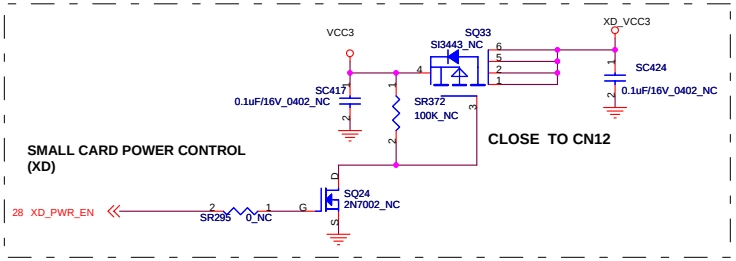
Elitegroup Computer Systems

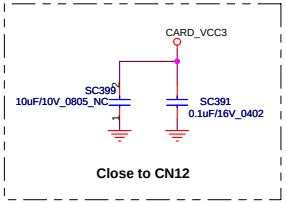
Title: G420_OZ128 1394 & CARD READER

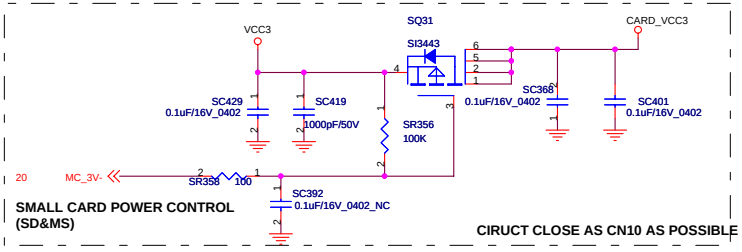
Size	Document Number	Rev
Custom	420 -1-4-01	3.0

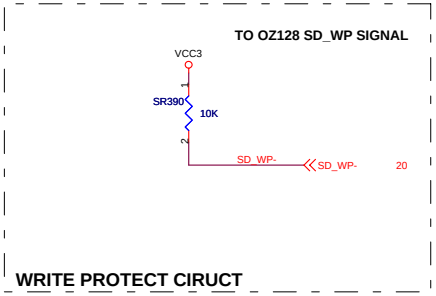
Date: Thursday, August 03, 2006 Sheet 20 of 44











CARD READER EC FUNCTION TABLE

	SD	SD LOCK	SD UNLOCK
XD_CD-	L	H	H
XD_PWR_EN (OUT)	H	L	L
SD_WP- (OUT)	H	H	H to L

Elitegroup Computer Systems

Title: **G420 CARDREADER CONNECT**

Size: Custom | Document Number: 420 -1-4-01 | Rev: 3.0

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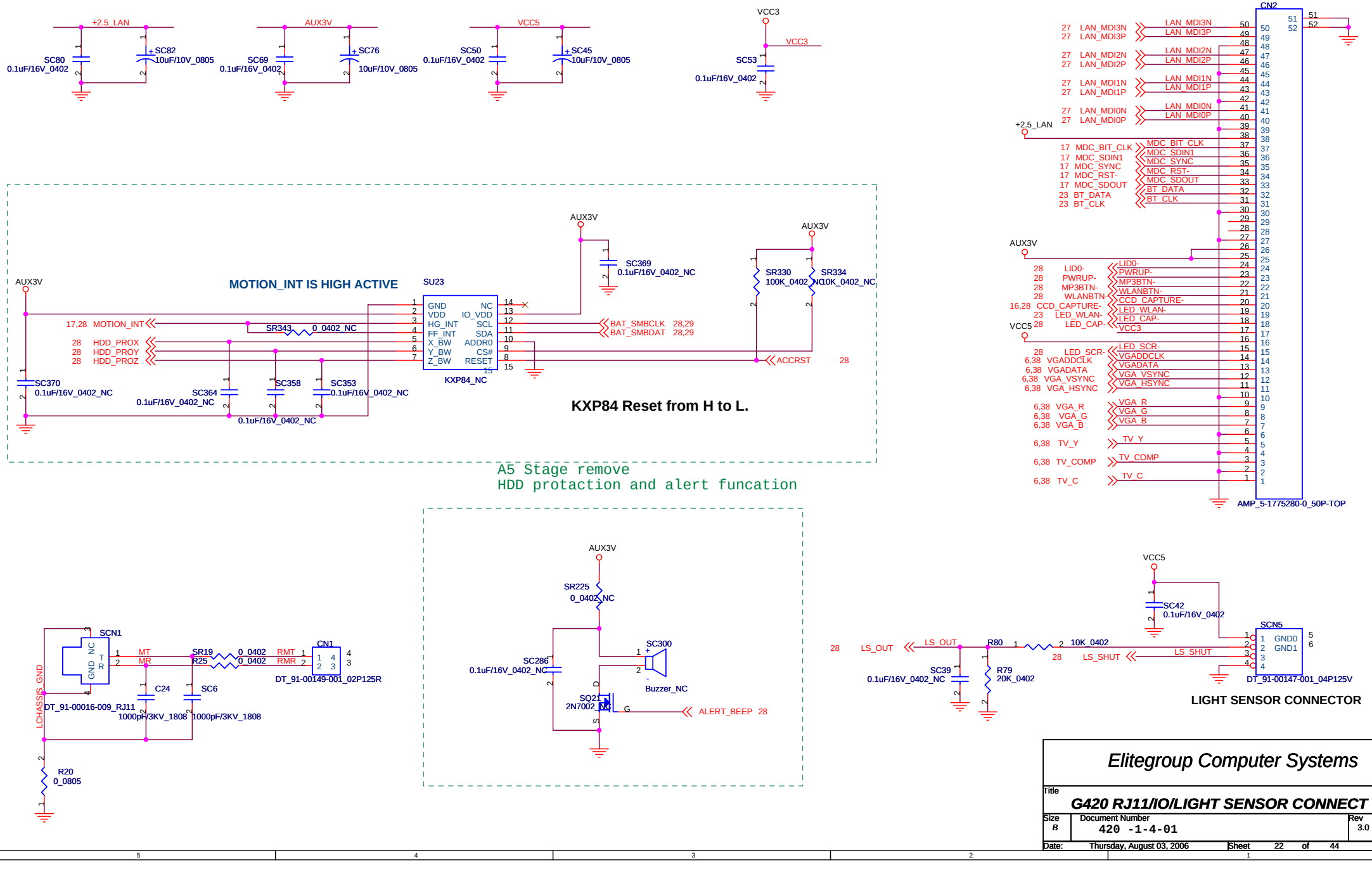

Elitegroup Computer Systems			
Title: G420 RJ11/IO/LIGHT SENSOR CONNECT			
Size: B	Document Number: 420 -1-4-01		Rev: 3.0
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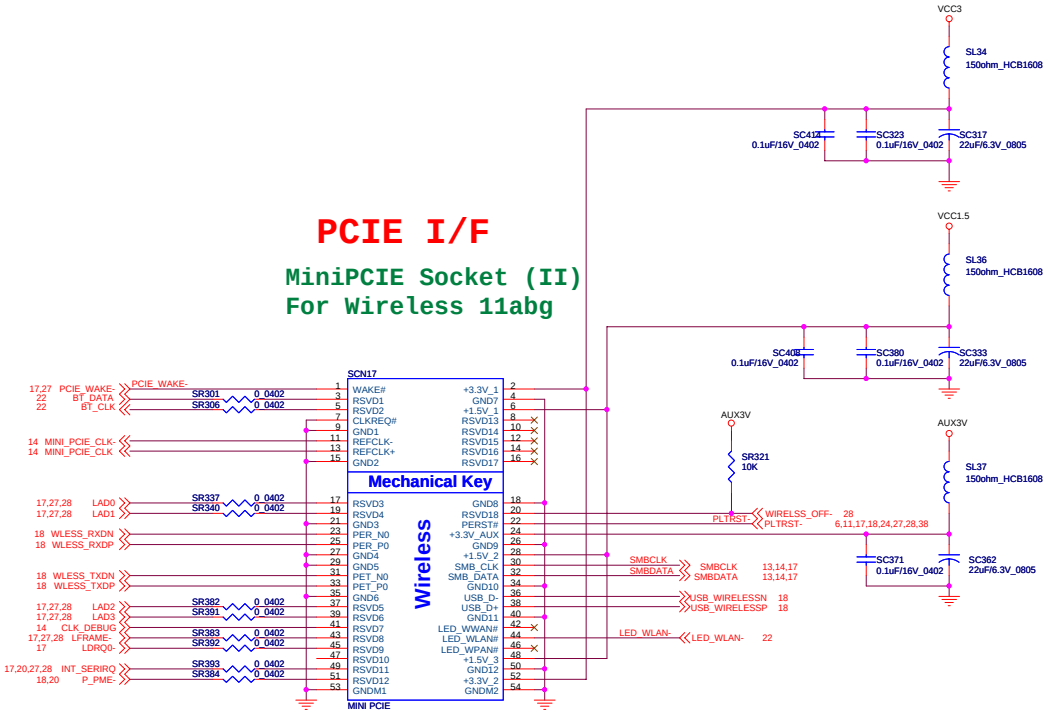
PCIE I/F

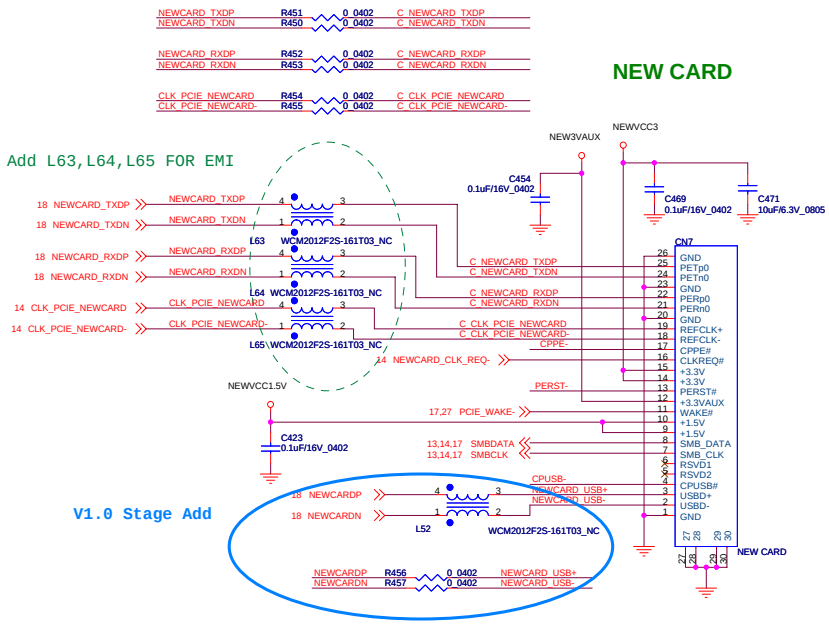
MiniPCIE Socket (II)
For Wireless 11abg

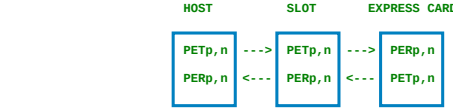


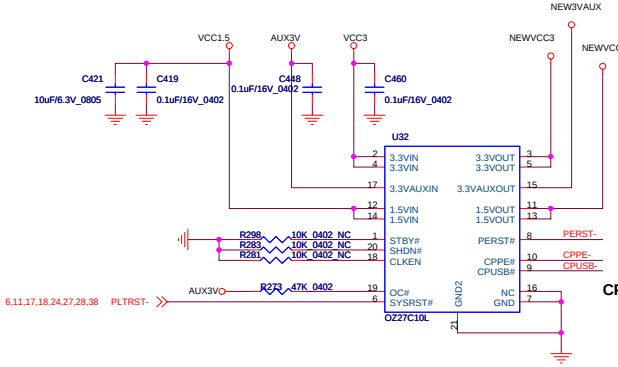
A5 Stage Add L63,L64,L65 FOR EMI

V1.0 Stage Add

NEW CARD







CPPE- and CPUSB- internal pull up.

Elitegroup Computer Systems			
Title: G420 MINI PCI TV TUNER			
Size: C	Document Number: 420 -1-4-01		Rev: 3.0
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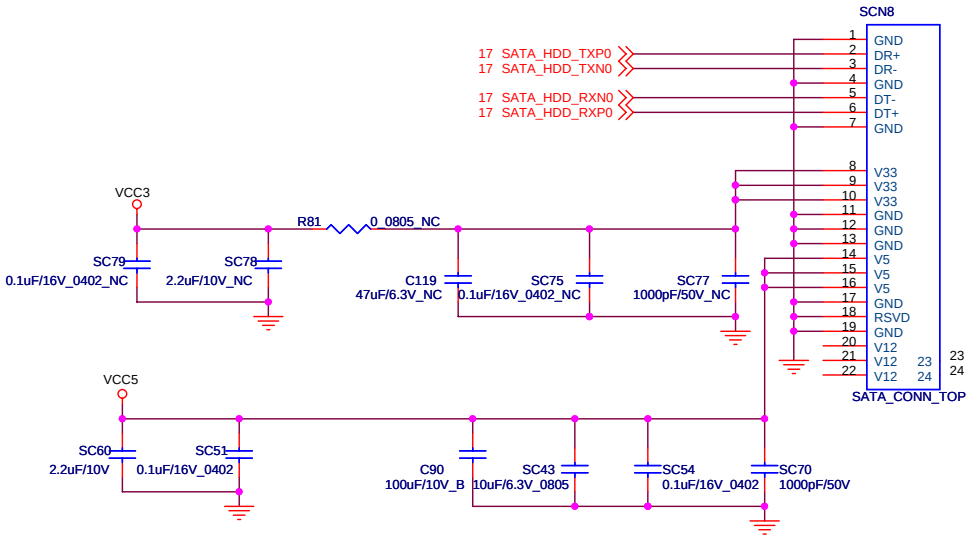
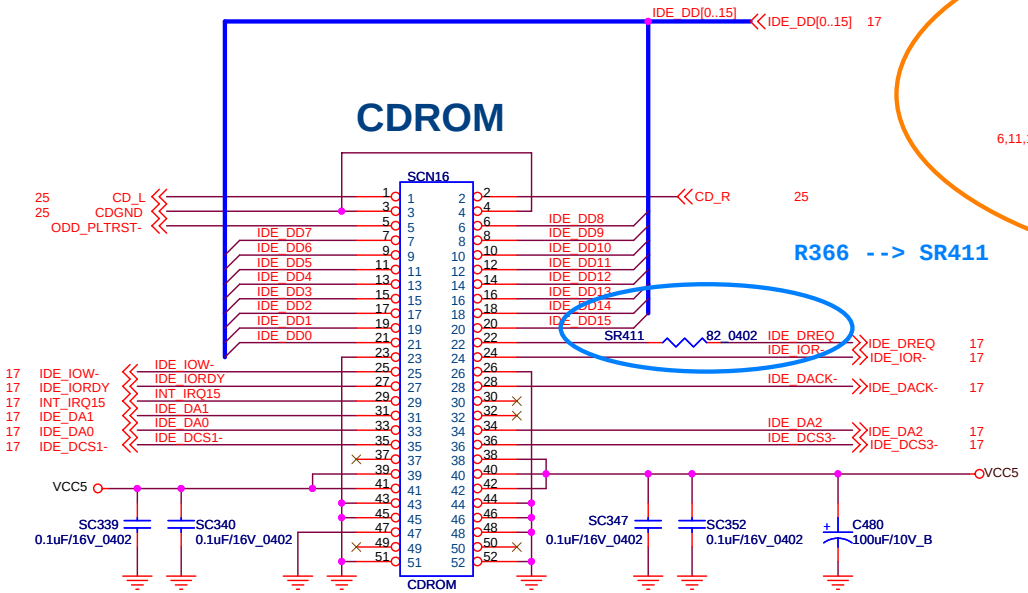
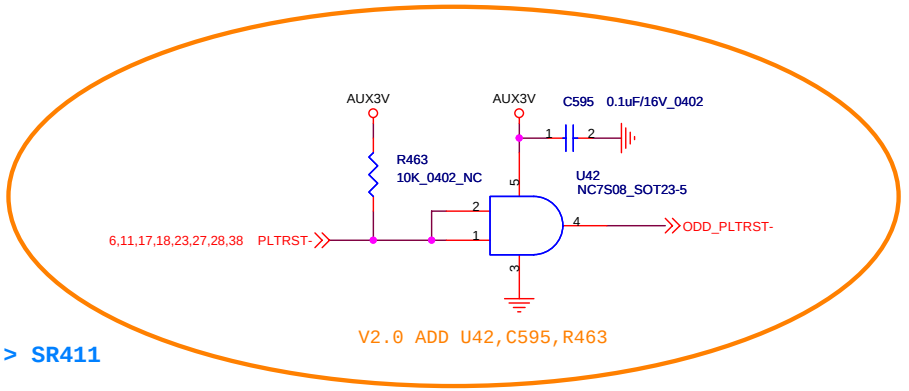
HDD



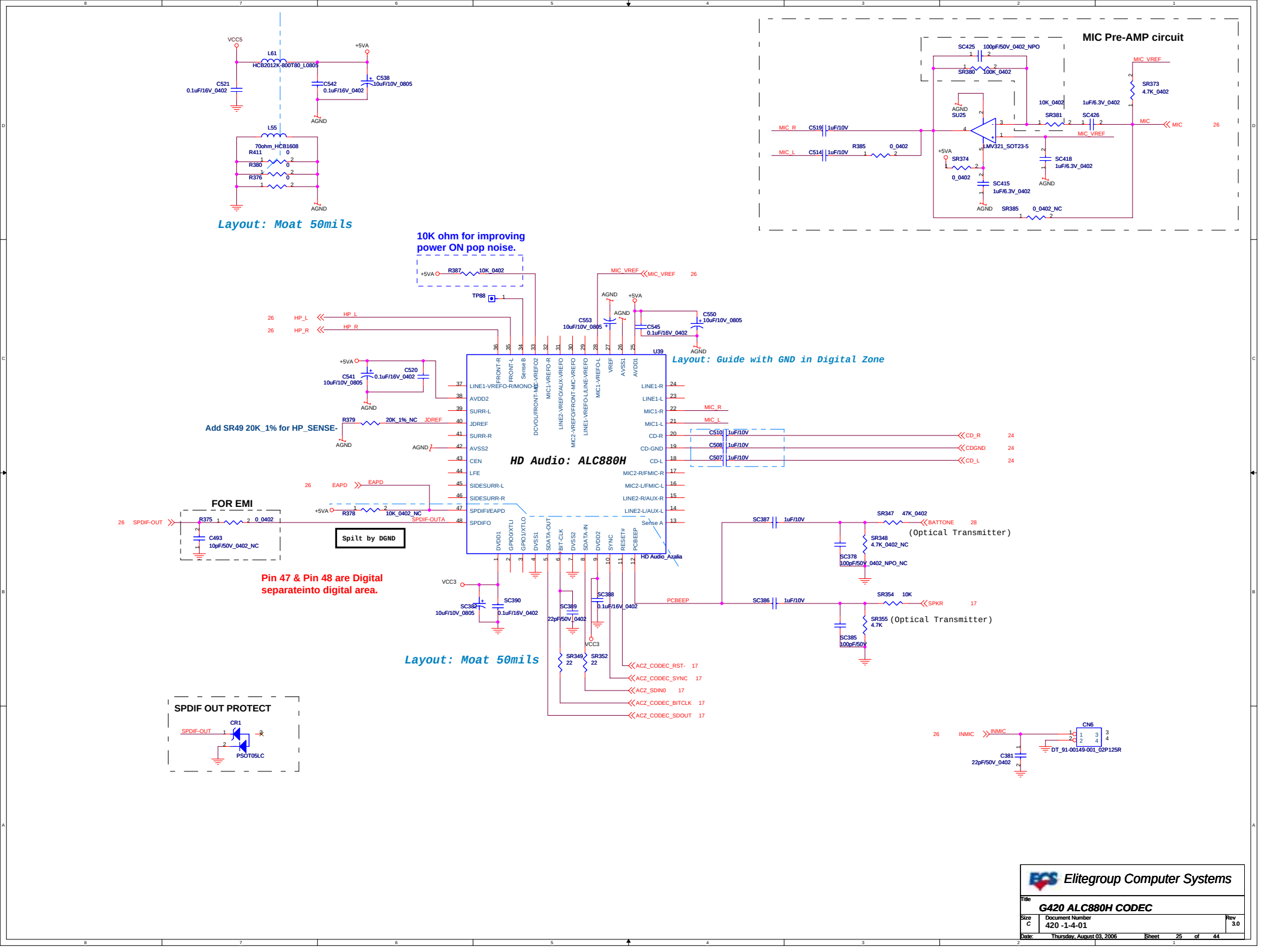
CDROM



R366 --> SR411



Elitegroup Computer Systems		
Title: G420 HDD & CDROM CONN		
Size: B	Document Number: 420 -1-4-01	Rev: 3.0
Date: Thursday, August 03, 2006	Sheet 24 of 44	


MIC Pre-AMP circuit
Layout: Moat 50mils
10K ohm for improving power ON pop noise.
Layout: Guide with GND in Digital Zone
HD Audio: ALC880H
Add SR49 20K_1% for HP_SENSE-
FOR EMI
Spilt by DGND
Pin 47 & Pin 48 are Digital separateinto digital area.
Layout: Moat 50mils
(Optical Transmitter)
(Optical Transmitter)
SPDIF OUT PROTECT
PSOT05LC
Elitegroup Computer Systems
G420 ALC880H CODEC
Document Number 420 -1-4-01
Rev 3.0
Thursday, August 03, 2006
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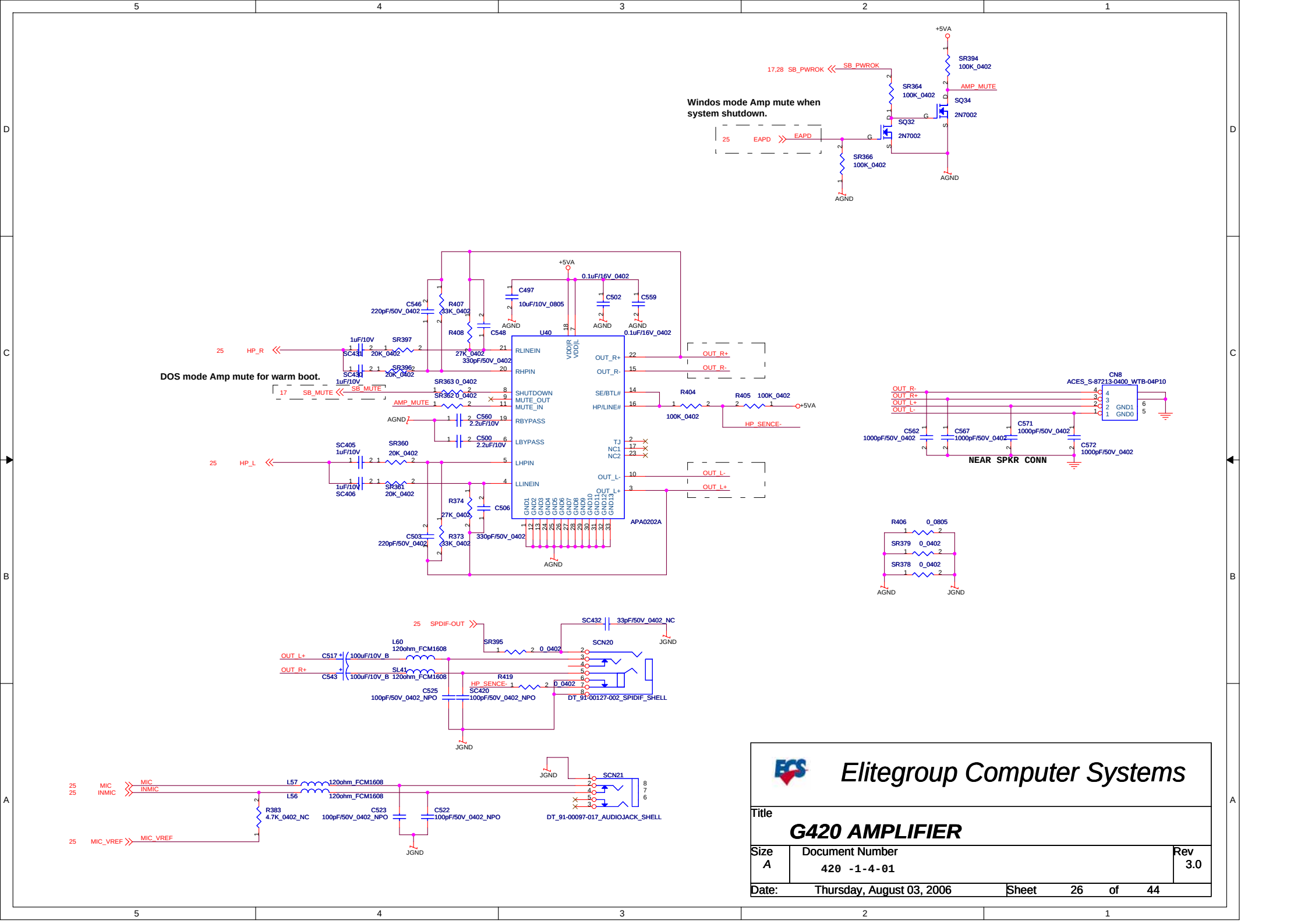
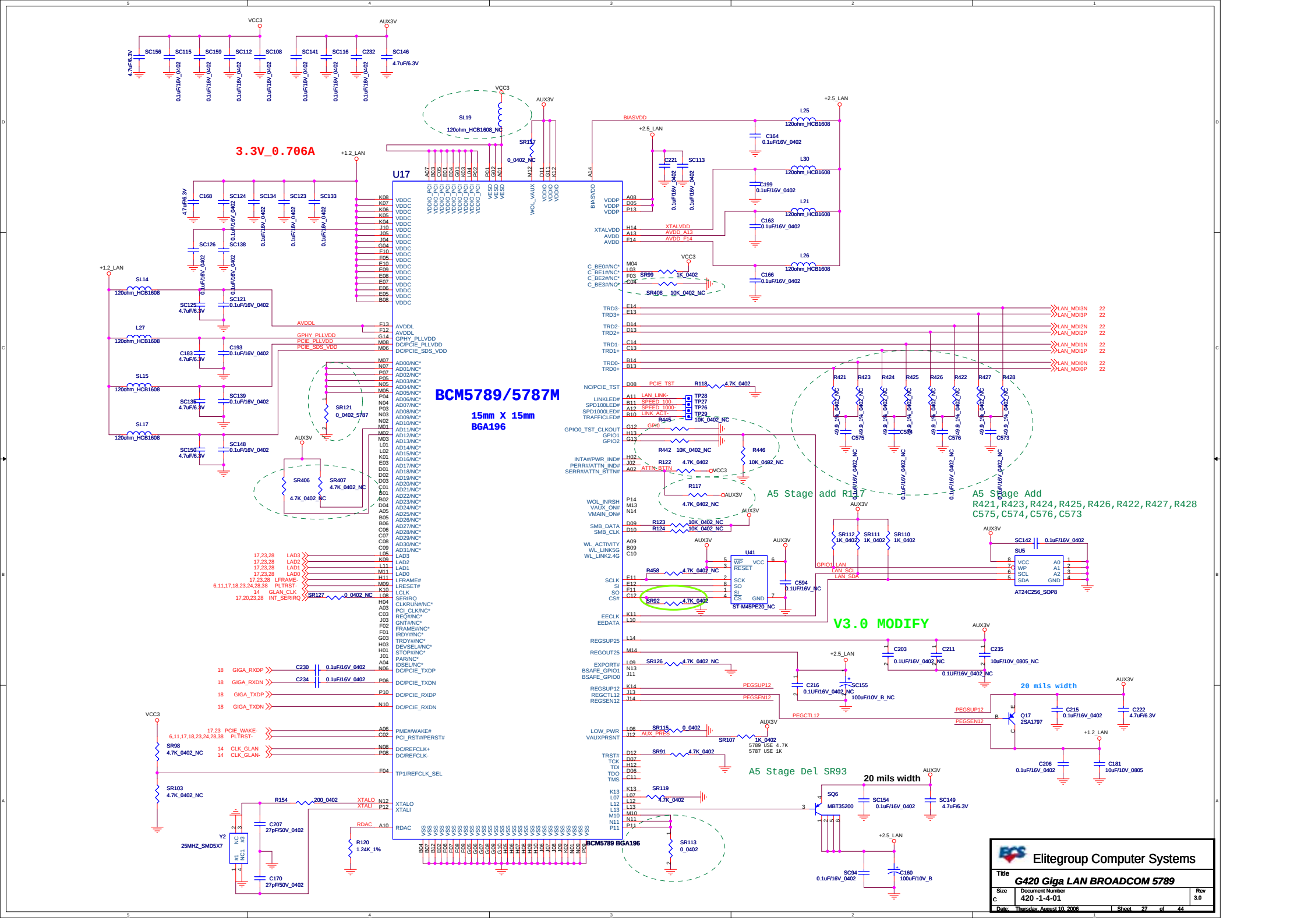
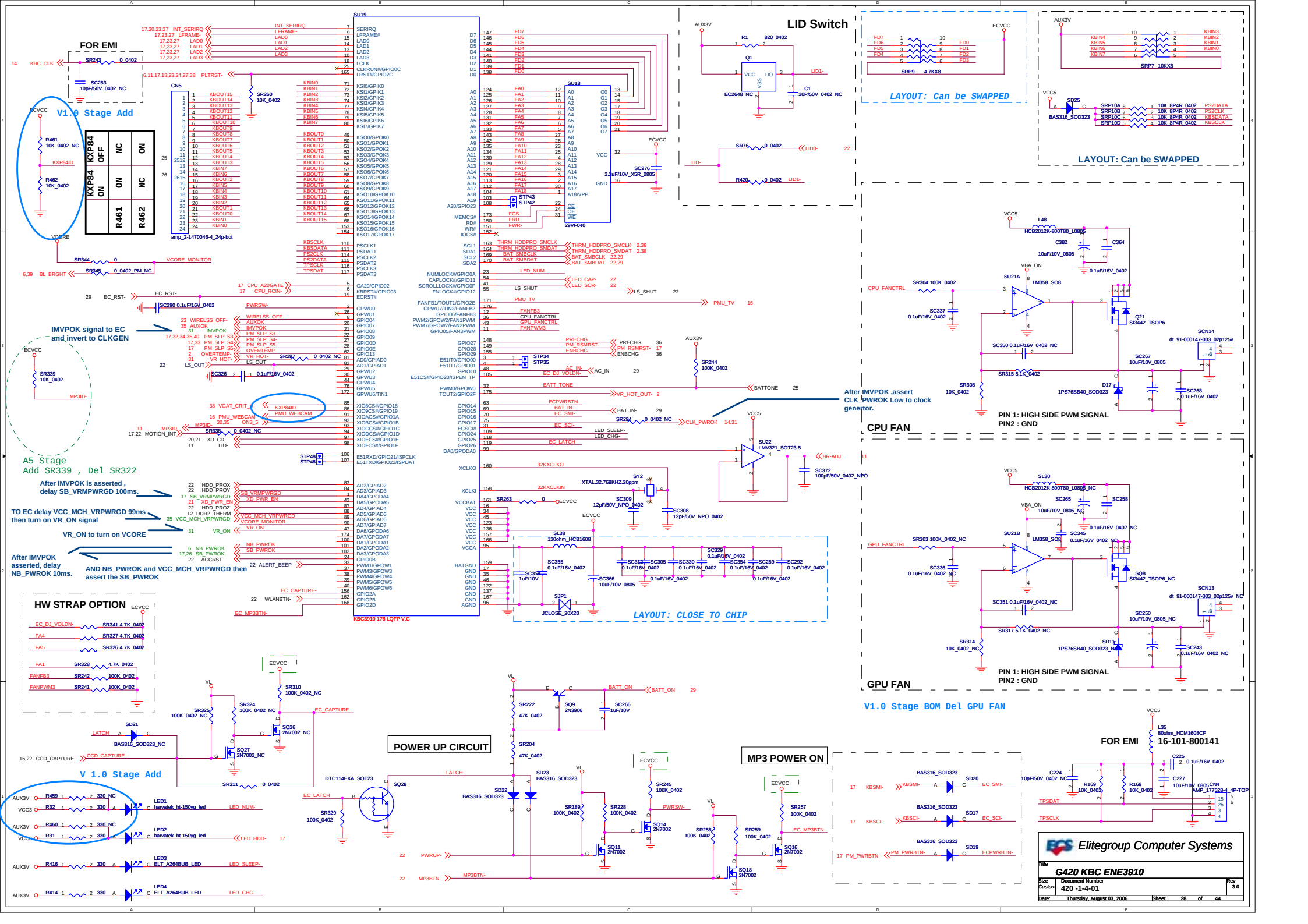

Windos mode Amp mute when system shutdown.
DOS mode Amp mute for warm boot.
NEAR SPKR CONN
Elitegroup Computer Systems
G420 AMPLIFIER
Size A
Document Number 420 -1-4-01
Rev 3.0
Date: Thursday, August 03, 2006
Sheet 26 of 44


3.3V_0.706A
U17
BCM5789/5787M
15mm X 15mm
BGA196
BCM5789 BGA196
A5 Stage add R117
A5 Stage Add
R421,R423,R424,R425,R426,R422,R427,R428
C575,C574,C576,C573
V3.0 MODIFY
A5 Stage Del SR93
20 mils width
20 mils width
Elitegroup Computer Systems
Title
G420 Giga LAN BROADCOM 5789
Size
C
Document Number
420 -1-4-01
Rev
3.0
Date: Thursday, August 10, 2006
Sheet 27 of 44


FOR EMI
V1.0 Stage Add
KXP84 OFF NC ON
KXP84 ON ON NC
R461 R462
A5 Stage
Add SR339 , Del SR322
IMVPOK signal to EC and invert to CLKGEN
After IMVPOK is asserted , delay SB_VRMPWRGD 100ms.
TO EC delay VCC_MCH_VRPWRGD 99ms then turn on VR_ON signal
VR_ON to turn on VCORE
After IMVPOK asserted, delay NB_PWROK 10ms.
AND NB_PWROK and VCC_MCH_VRPWRGD then assert the SB_PWROK
HW STRAP OPTION
V 1.0 Stage Add
LED1 harvatek ht-150yg led
LED2 harvatek ht-150yg led
LED3 ELT A264BUB LED
LED4 ELT A264BUB LED
POWER UP CIRCUIT
LID Switch
LAYOUT: Can be SWAPPED
LAYOUT: Can be SWAPPED
LAYOUT: CLOSE TO CHIP
After IMVPOK ,assert CLK_PWROK Low to clock genertor.
CPU FAN
PIN 1: HIGH SIDE PWM SIGNAL
PIN2 : GND
GPU FAN
PIN 1: HIGH SIDE PWM SIGNAL
PIN2 : GND
V1.0 Stage BOM Del GPU FAN
MP3 POWER ON
FOR EMI
16-101-800141
KBC3910 176 LQFP V.C
amp_2-1470046-4_24p-bot
Elitegroup Computer Systems
G420 KBC ENE3910
Document Number 420 -1-4-01
Rev 3.0
Thursday, August 03, 2006
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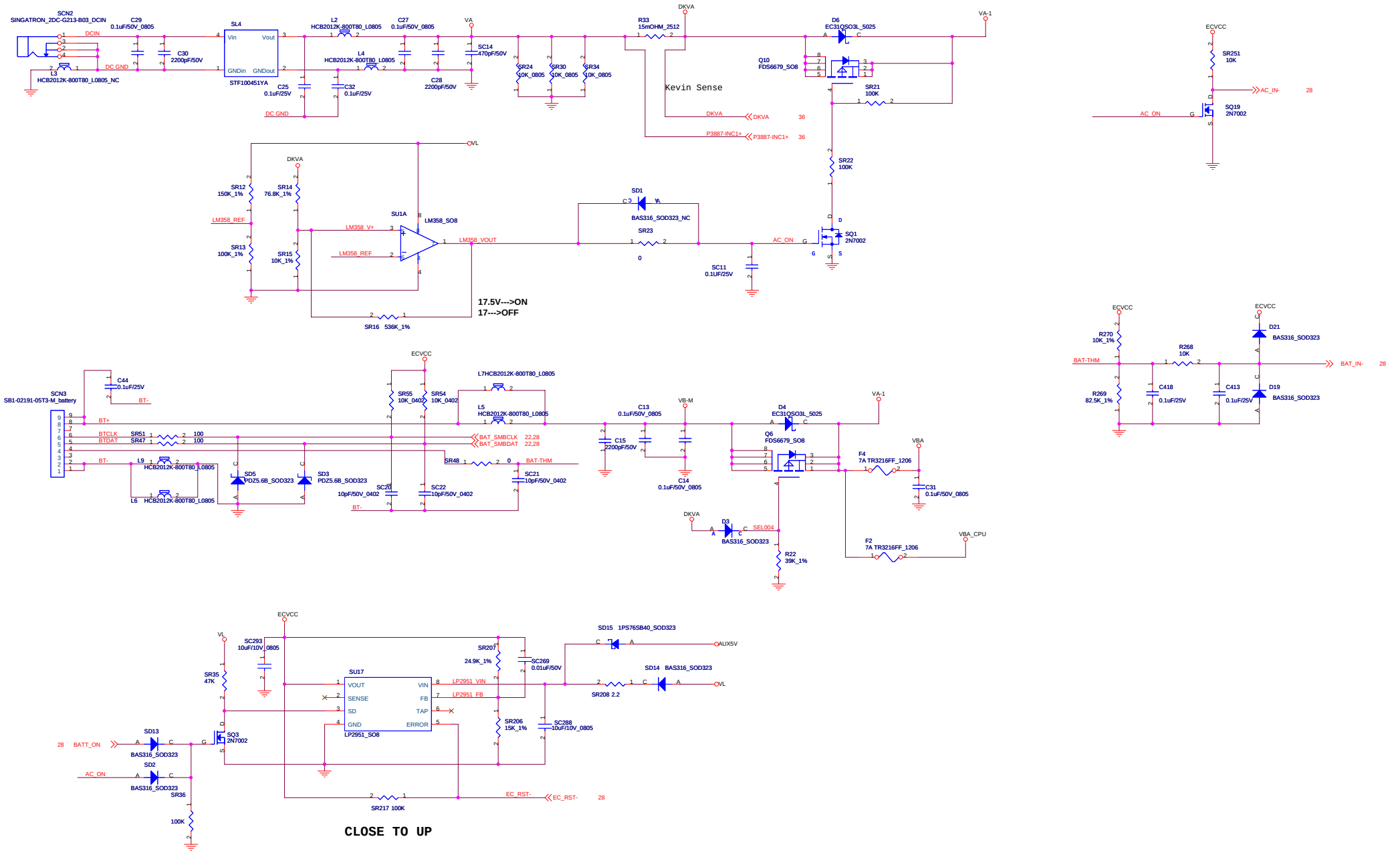
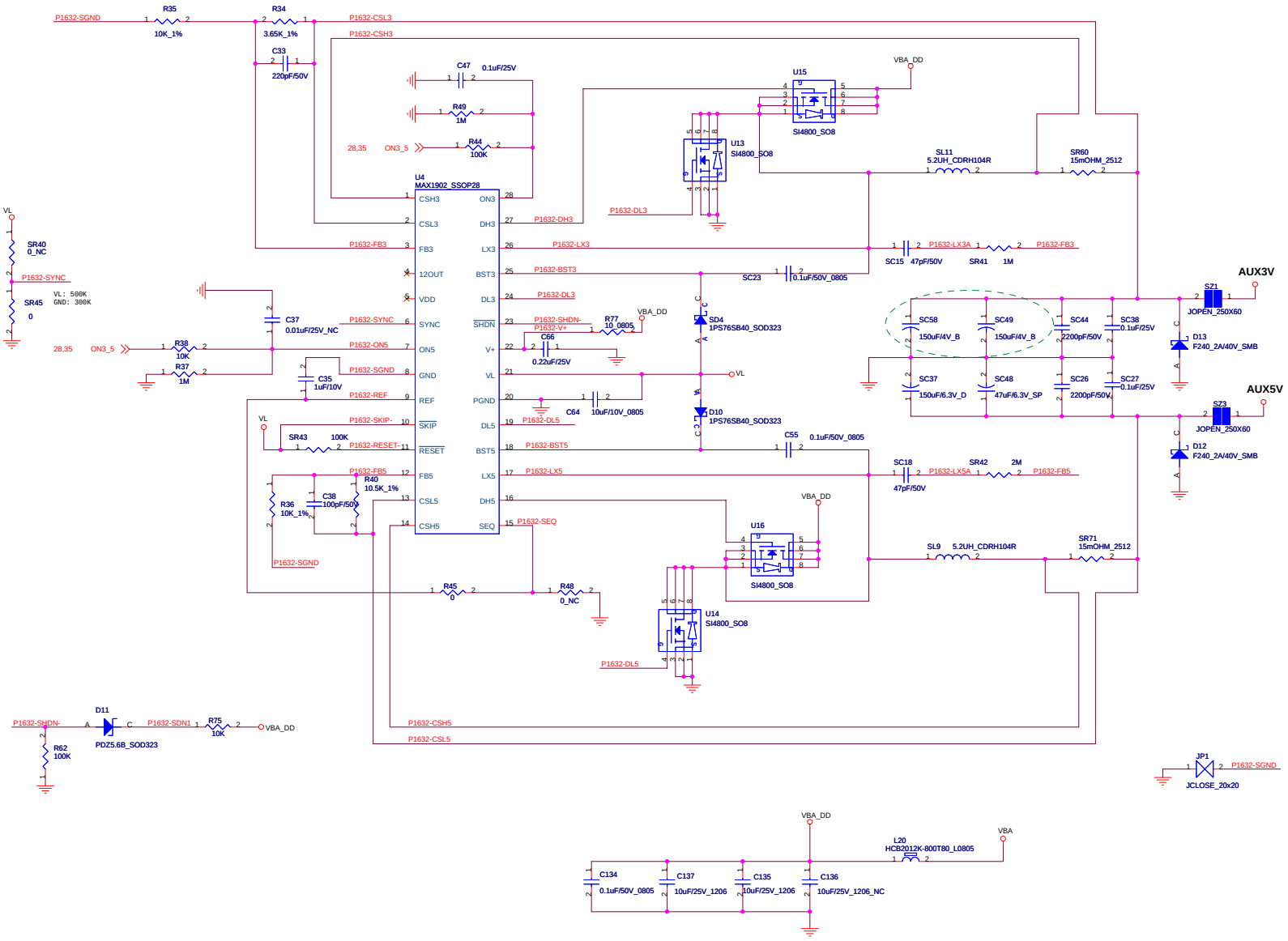


Elitegroup Computer Systems

Title: G420 DC IN & BATT CONN

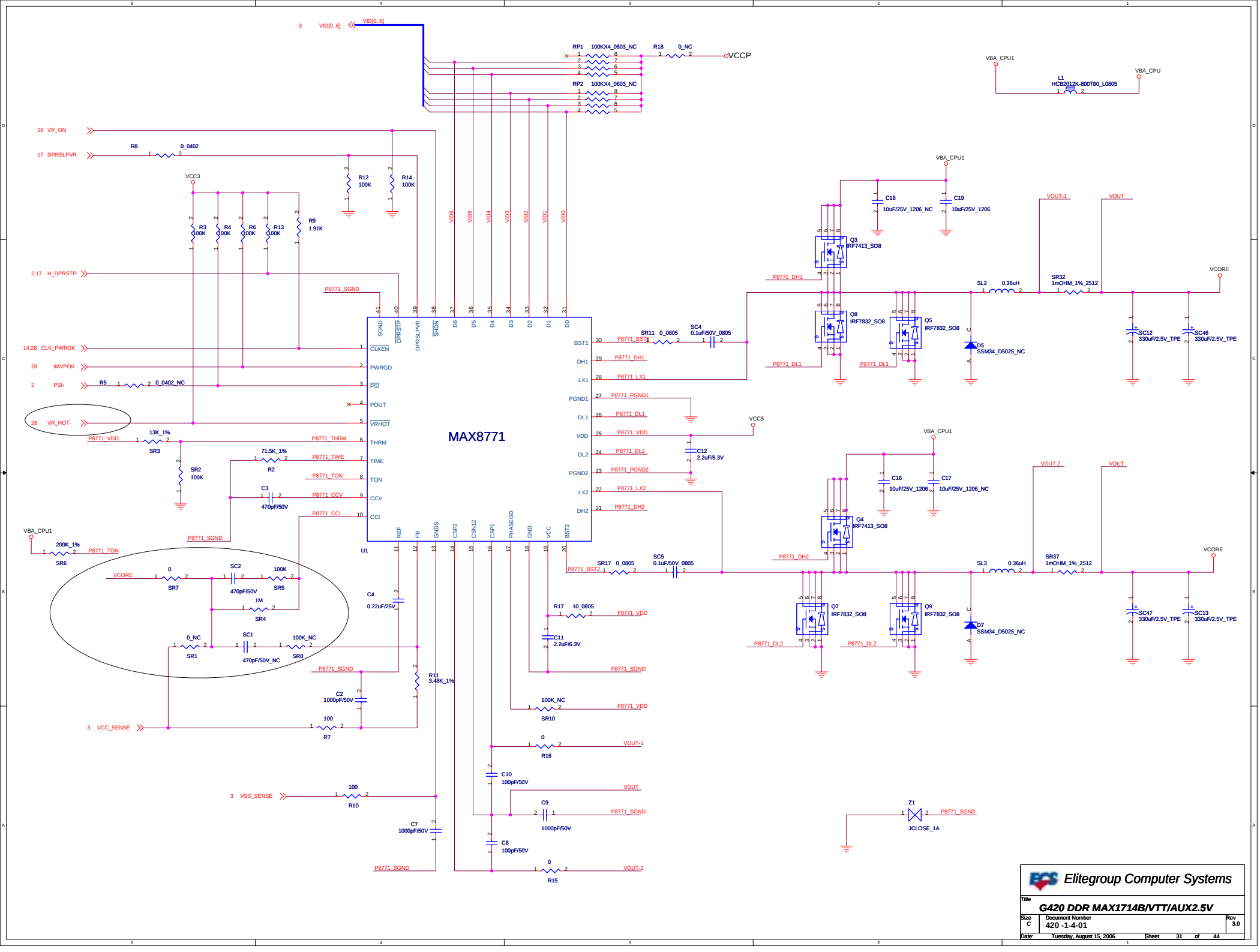
Size: Custom | Document Number: 420 -1-4-01 | Rev: 3.0

Date: Thursday, August 03, 2006 | Sheet 29 of 44

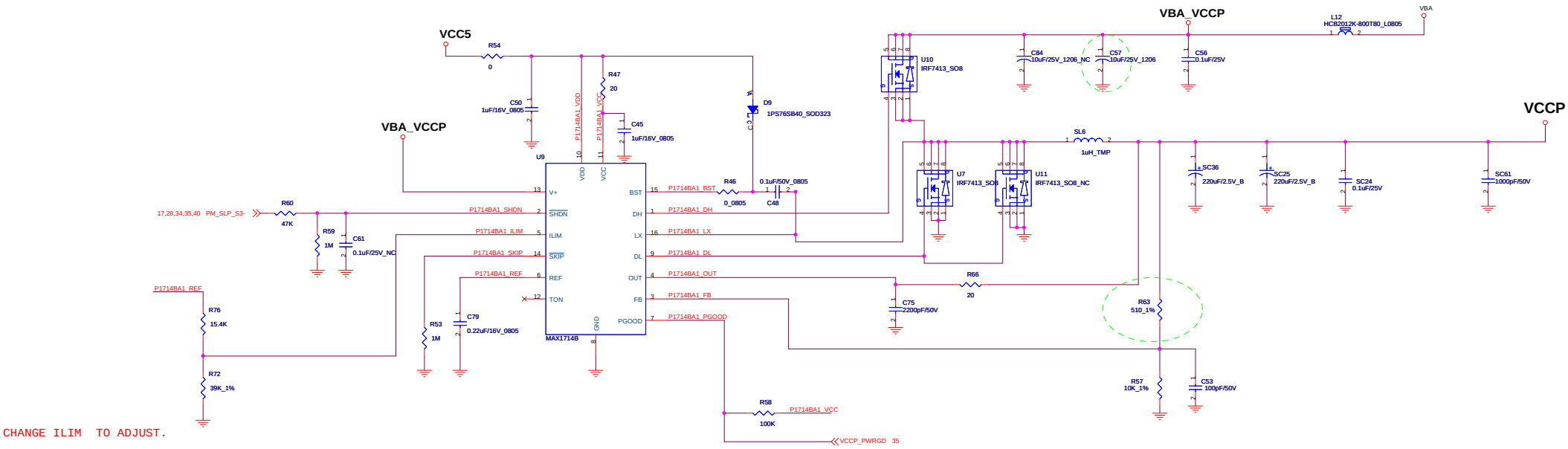


Elitegroup Computer Systems

Title	G420 AUX5V/AUX3V MAX1902	
Size C	Document Number 420 -1-4-01	Rev 3.0
Date: Tuesday, August 15, 2006	Sheet 30 of 44	



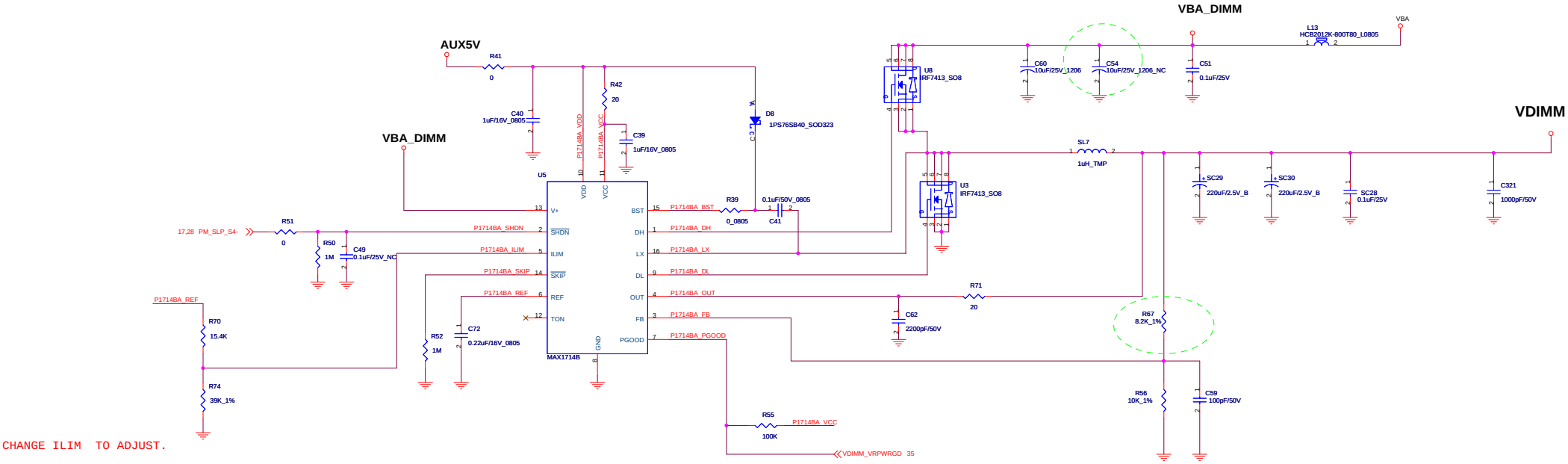
Elitegroup Computer Systems			
Title: G420 DDR MAX1714B/VTT/AUX2.5V			
Size: C	Document Number: 420 -1-4-01		Rev: 3.0
Date: Tuesday, August 15, 2006	Sheet 31 of 44		



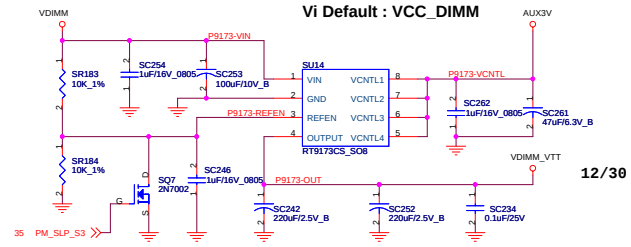
CHANGE ILIM TO ADJUST.

Elitegroup Computer Systems

Title	G420 MAX1714B_VCCP1.05V	
Size: Custom	Document Number: 420 -1-4-01	Rev: 3.0
Date: Tuesday, August 15, 2006	Sheet 32 of 44	

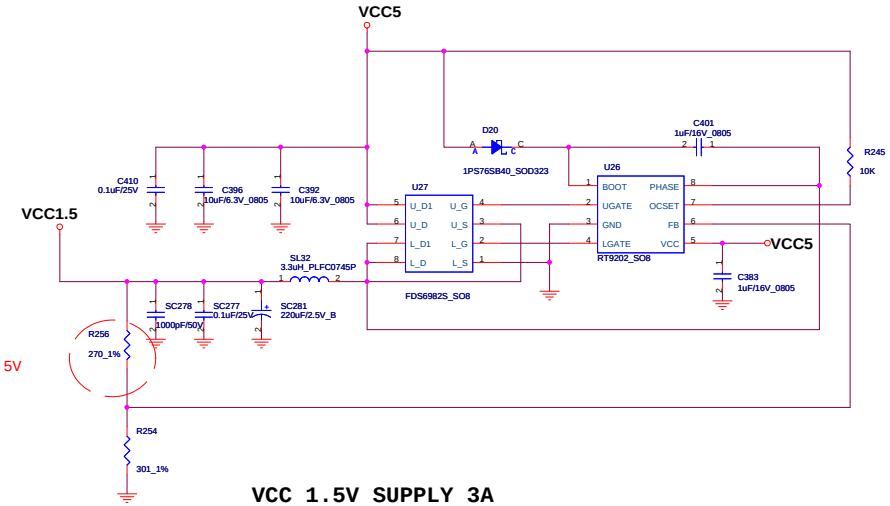


CHANGE ILIM TO ADJUST.



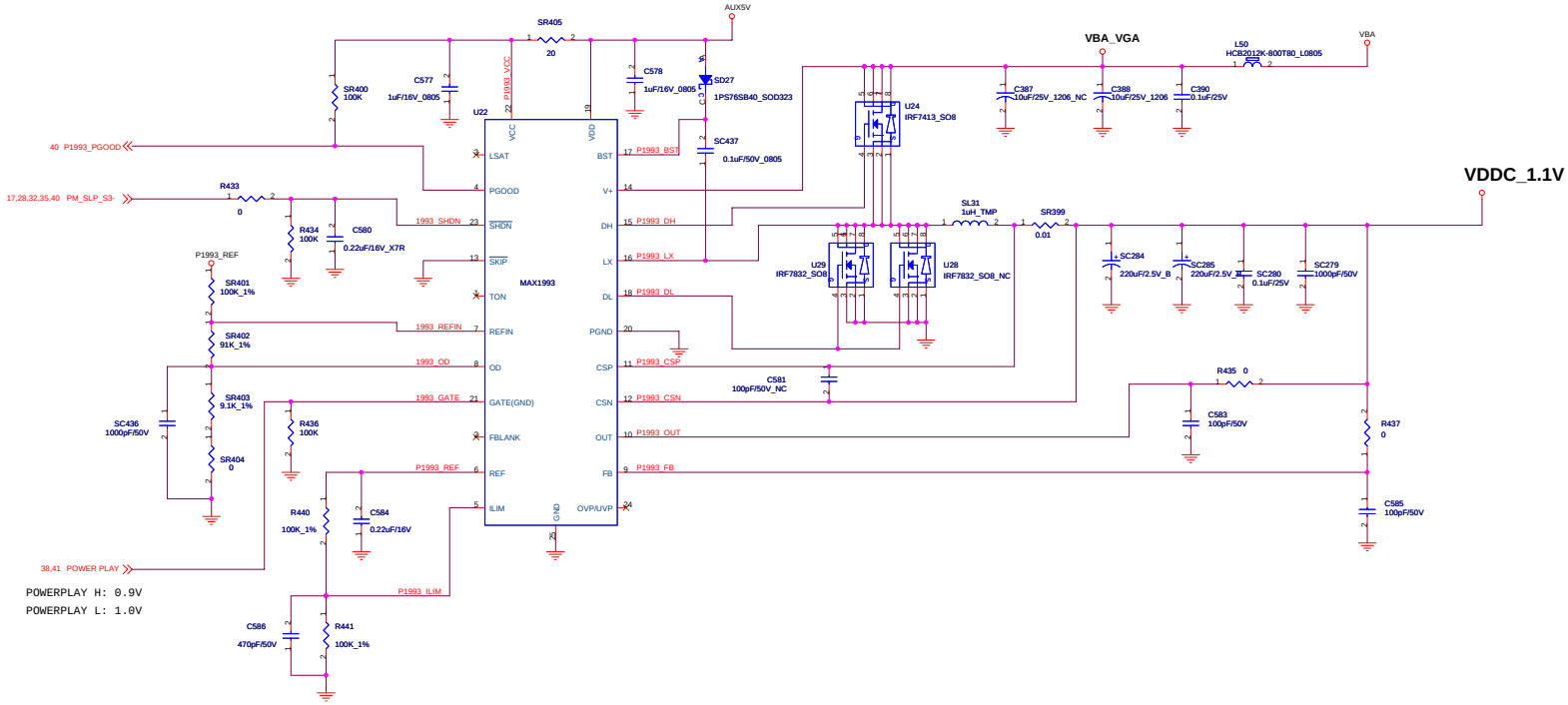
DIMM_1.8V SUPPLY 3.5A & VTT0.9V 1A FOR DDR

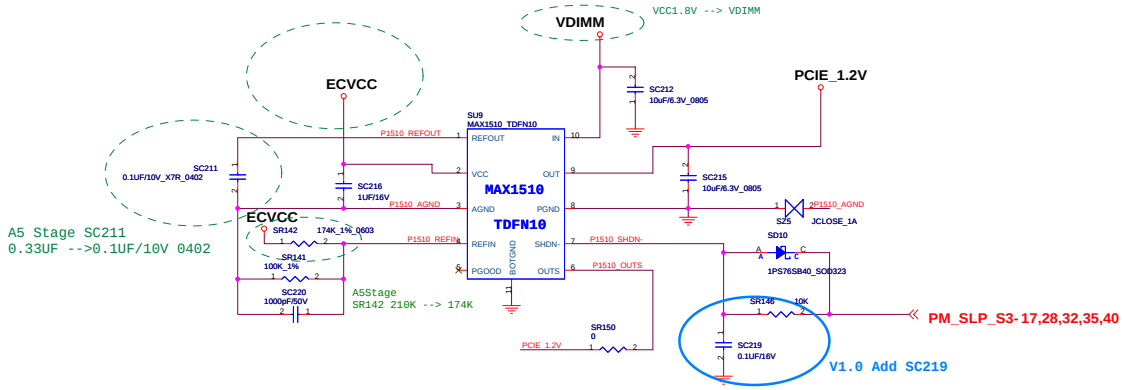
R256=270 OHM VOUT=1.5V



VCC 1.5V SUPPLY 3A

Elitegroup Computer Systems	
Title	G420 MAX1714B_VCCDIMM/VCC1.5V
Size: Custom	Document Number: 420 -1-4-01
Rev	3.0
Date: Tuesday, August 15, 2006	Sheet 33 of 44

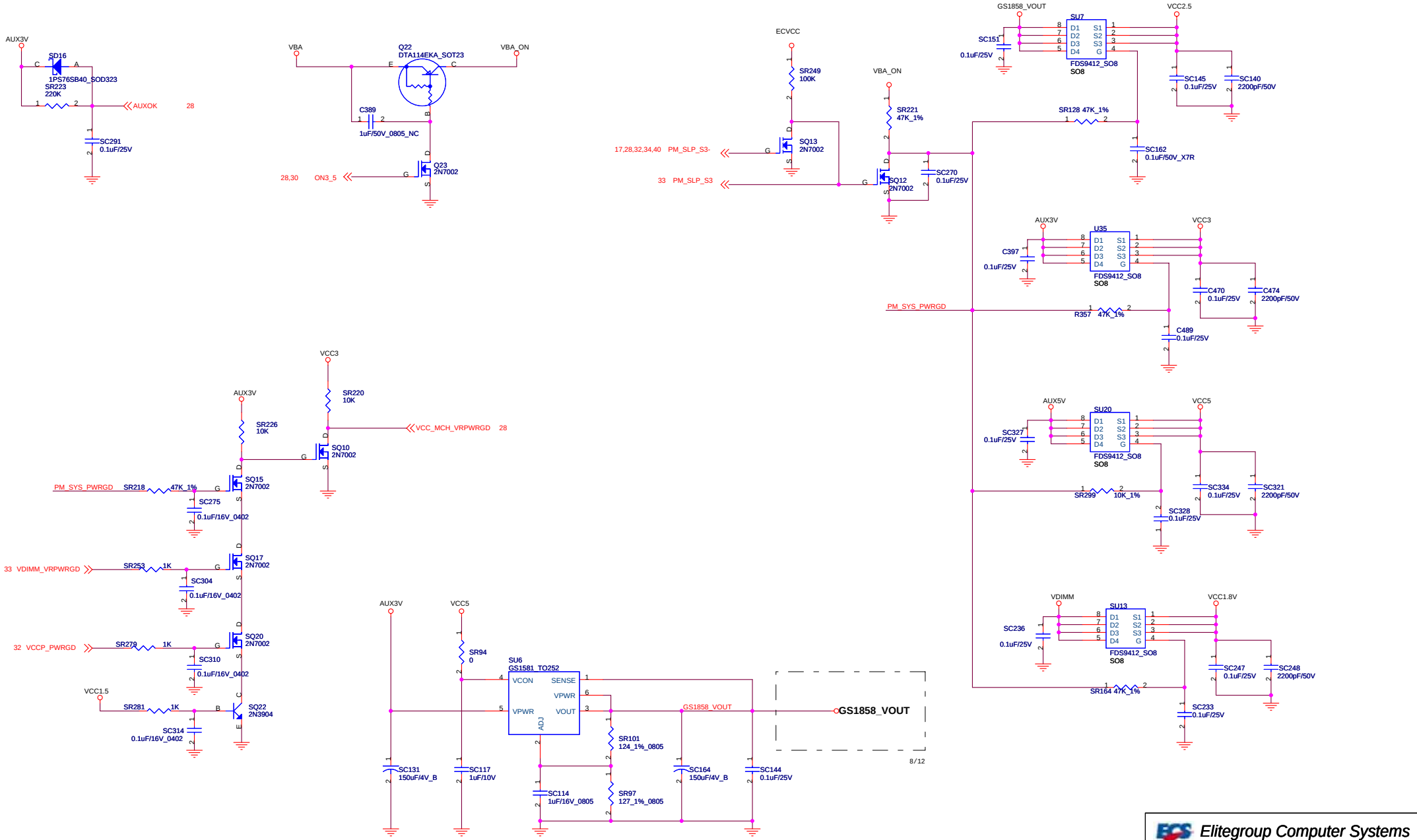




PCIE_1.2V FOR ATI 2A

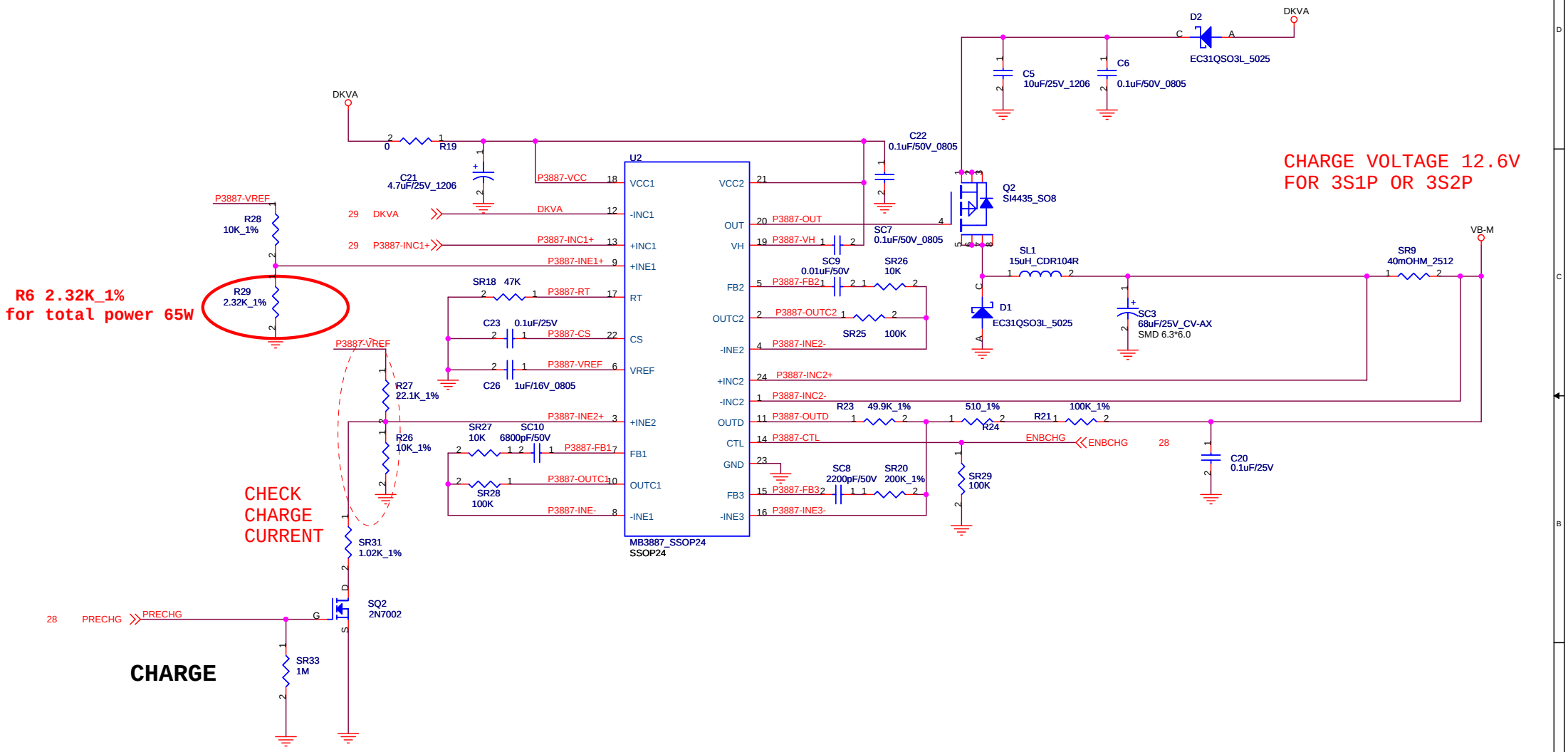
Elitegroup Computer Systems

Title: G420 STRAPS		
Size: Custom	Document Number: 420 -1-4-01	Rev: 3.0
Date: Tuesday, August 15, 2006	Sheet 34 of 44	

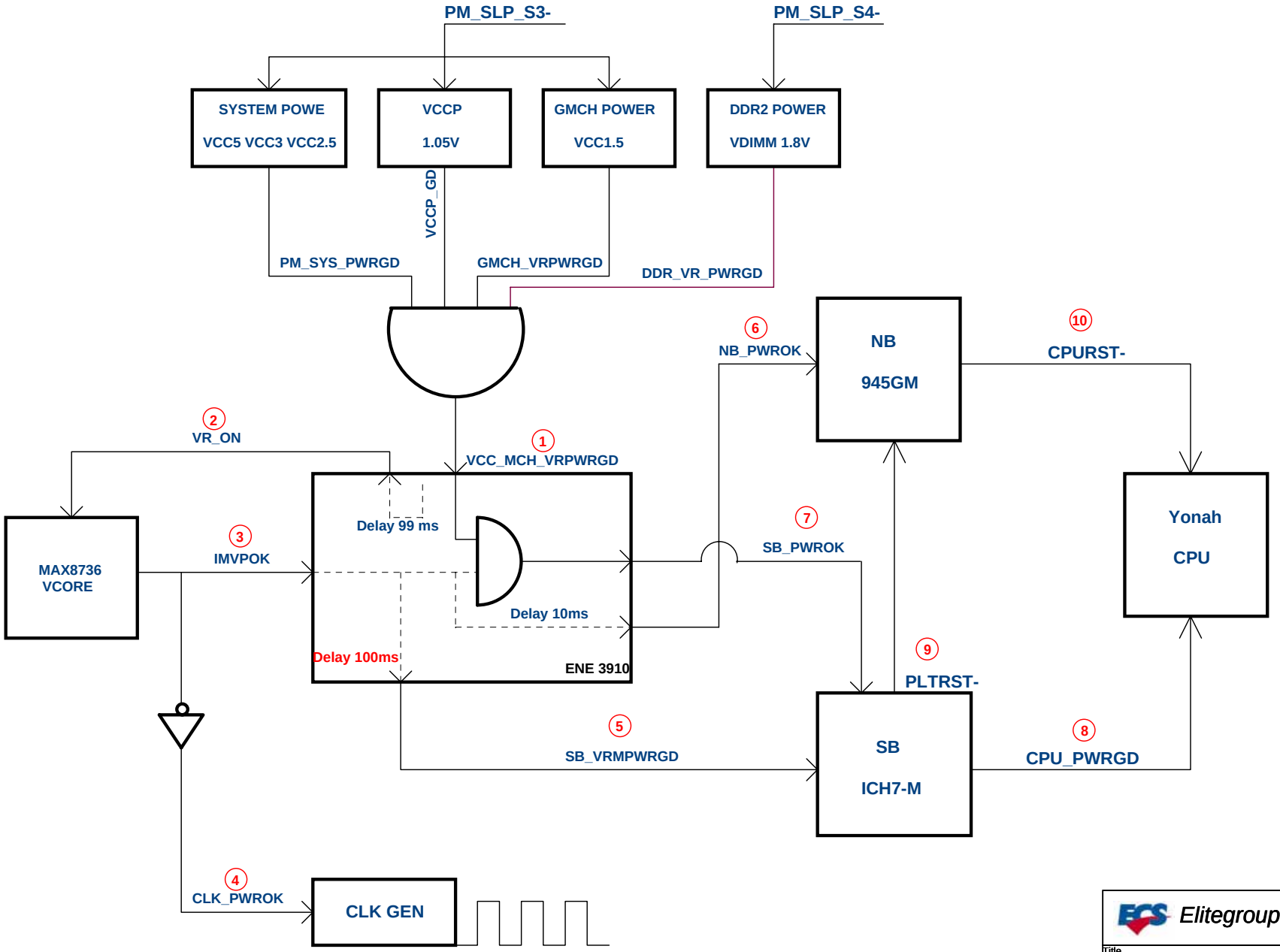


Elitegroup Computer Systems

Title	G420 POWER SW/VCC2.5	
Size: Custom	Document Number: 420 -1-4-01	Rev: 3.0
Date: Thursday, August 03, 2006	Sheet 35 of 44	



Elitegroup Computer Systems			
Title: G420 CHARGER CIRCUIT			
Size: B	Document Number: 420 -1-4-01		Rev: 3.0
Date: Thursday, August 03, 2006	Sheet 36 of 44		

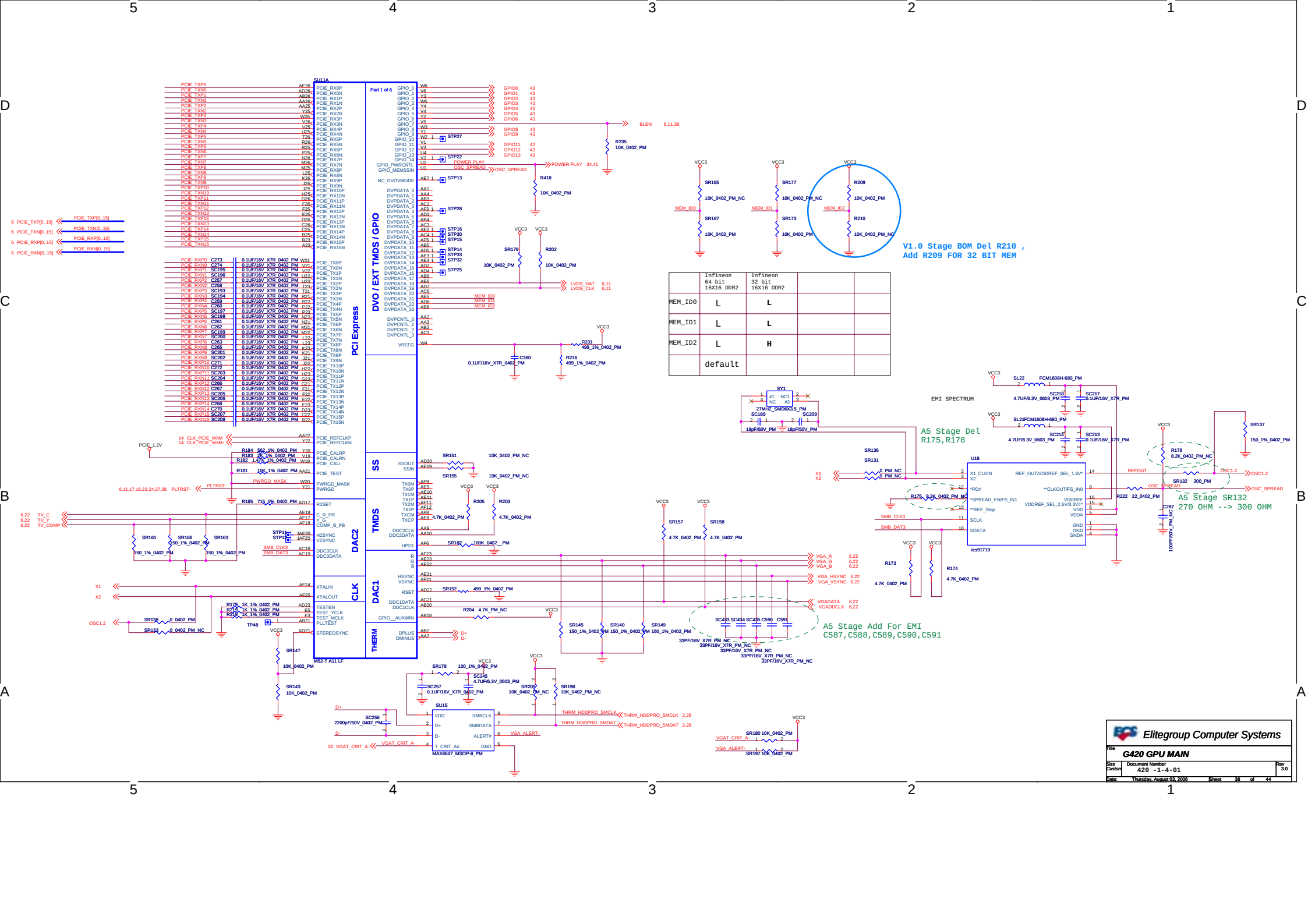


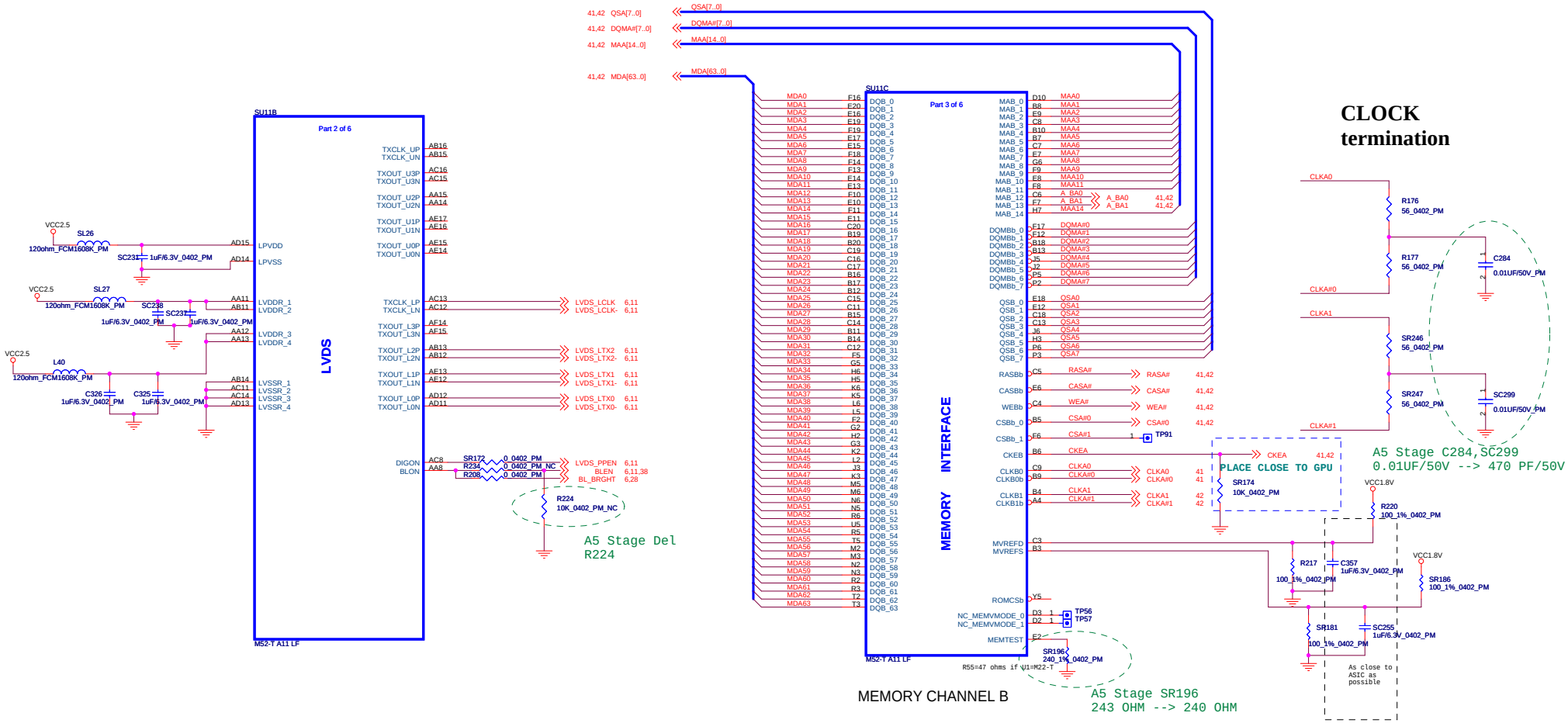
Elitegroup Computer Systems

Title: G420 POWER SEQUENCE

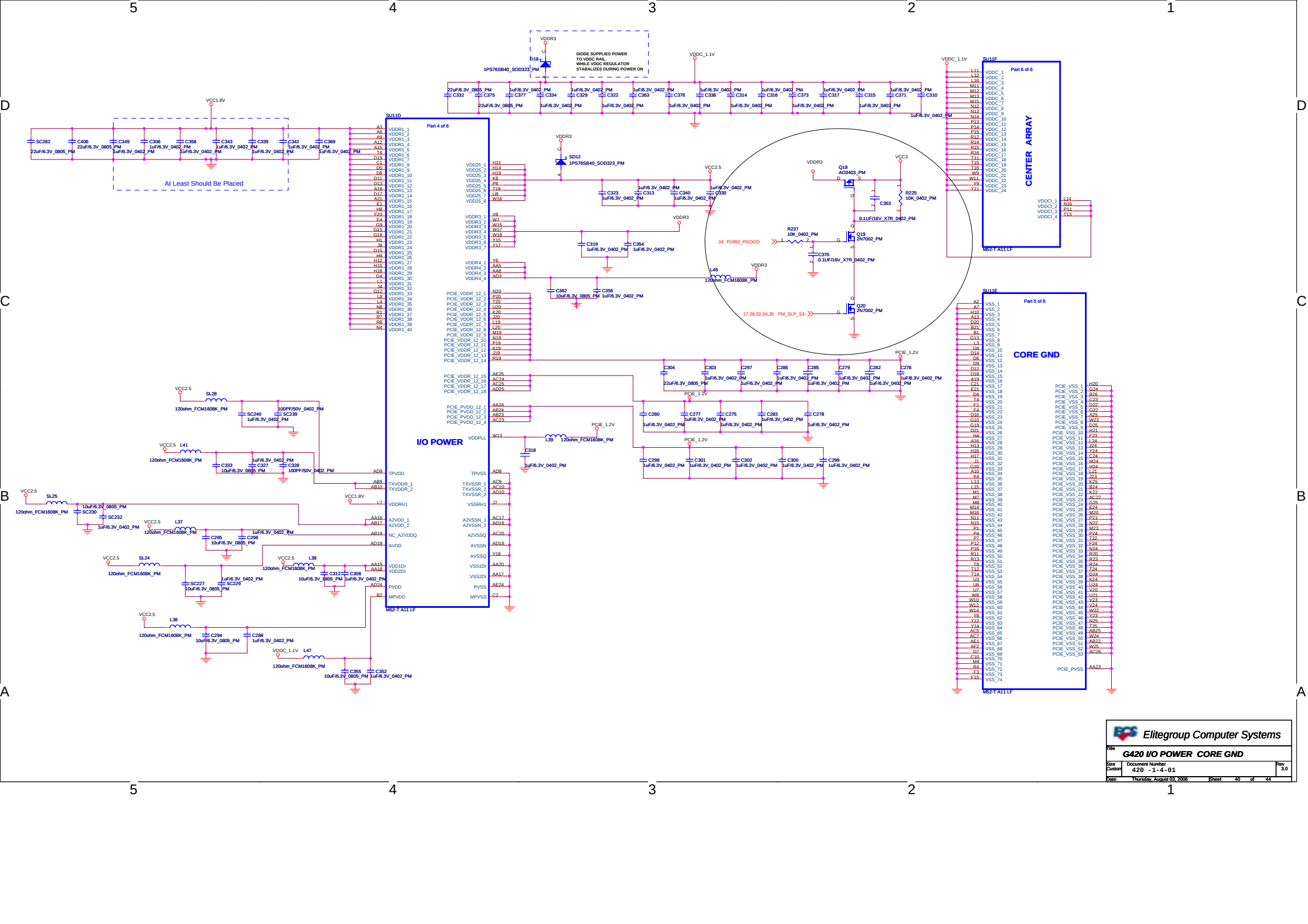
Size	Document Number	Rev
B	420 -1-4-01	3.0

Date: Thursday, August 03, 2006 Sheet 37 of 44


SU11A
PCI Express
DVO / EXT TMDS / GPIO
SS
TMDS
DAC2
CLK
DAC1
THERM
M52-T A11 LF
V1.0 Stage BOM Del R210 ,
Add R209 FOR 32 BIT MEM
Infineon 64 bit 16X16 DDR2
Infineon 32 bit 16X16 DDR2
MEM_ID0 L L
MEM_ID1 L L
MEM_ID2 L H
default
A5 Stage Del
R175,R178
A5 Stage SR132
270 OHM --> 300 OHM
A5 Stage Add For EMI
C587,C588,C589,C590,C591
EMI SPECTRUM
ics91719
MAX6647_MSOP-8_PM
Elitegroup Computer Systems
G420 GPU MAIN
Document Number 420 -1-4-01
Rev 3.0
Thursday, August 03, 2006
Sheet 38 of 44



Elitegroup Computer Systems			
Title	G420 MEMORY INTERFACE		
Size C	Document Number 420 -1-4-01		Rev 3.0
Date: Thursday, August 03, 2006	Sheet 39 of 44		


DIODE SUPPLIES POWER TO VDDC RAIL WHILE VDDC REGULATOR STABALIZES DURING POWER ON
At Least Should Be Placed
I/O POWER
CENTER ARRAY
CORE GND
Part 4 of 6
Part 5 of 6
Part 6 of 6
M52-T A11 LF
Elitegroup Computer Systems
G420 I/O POWER CORE GND
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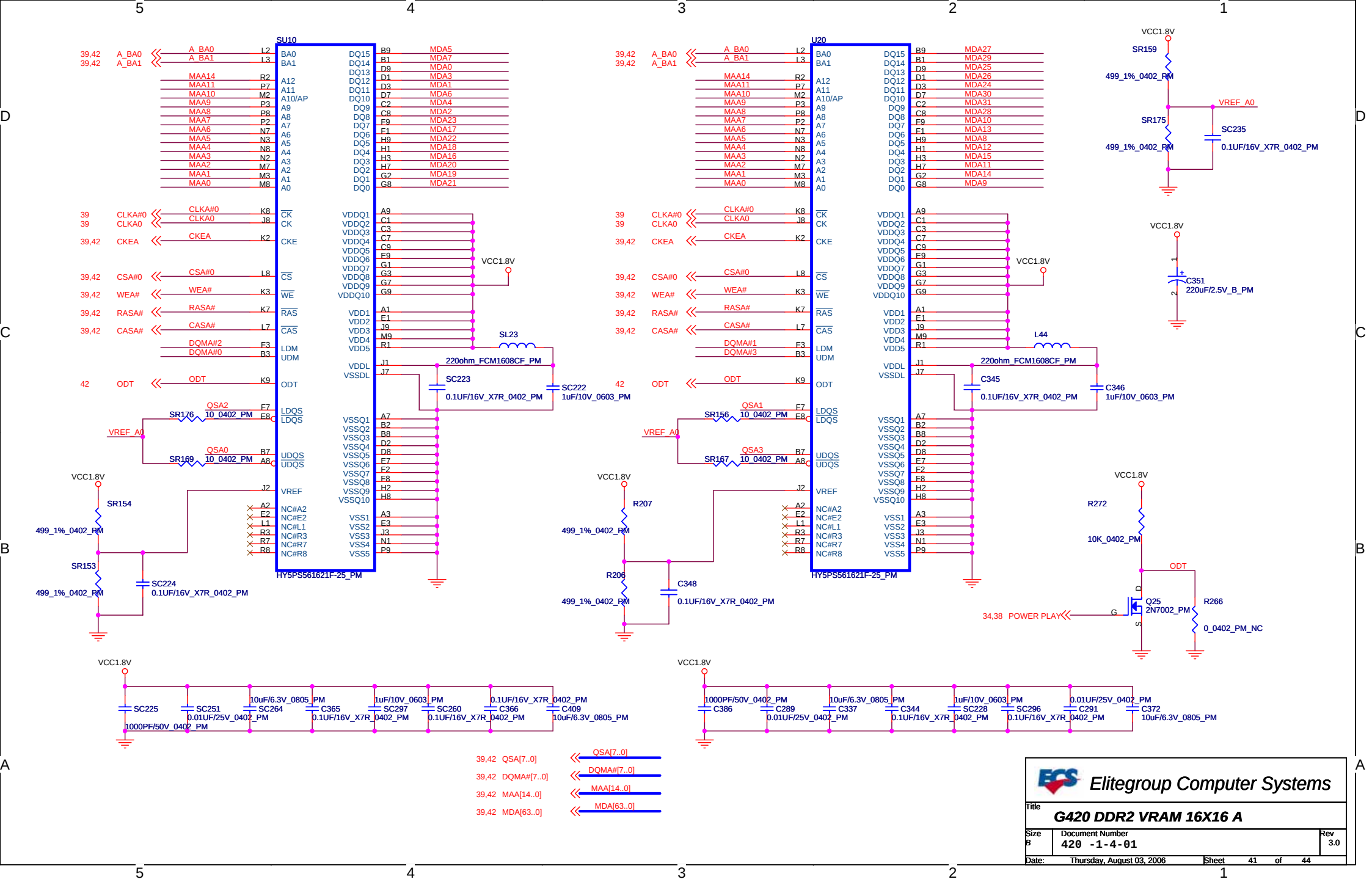

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Title: G420 DDR2 VRAM 16X16 A

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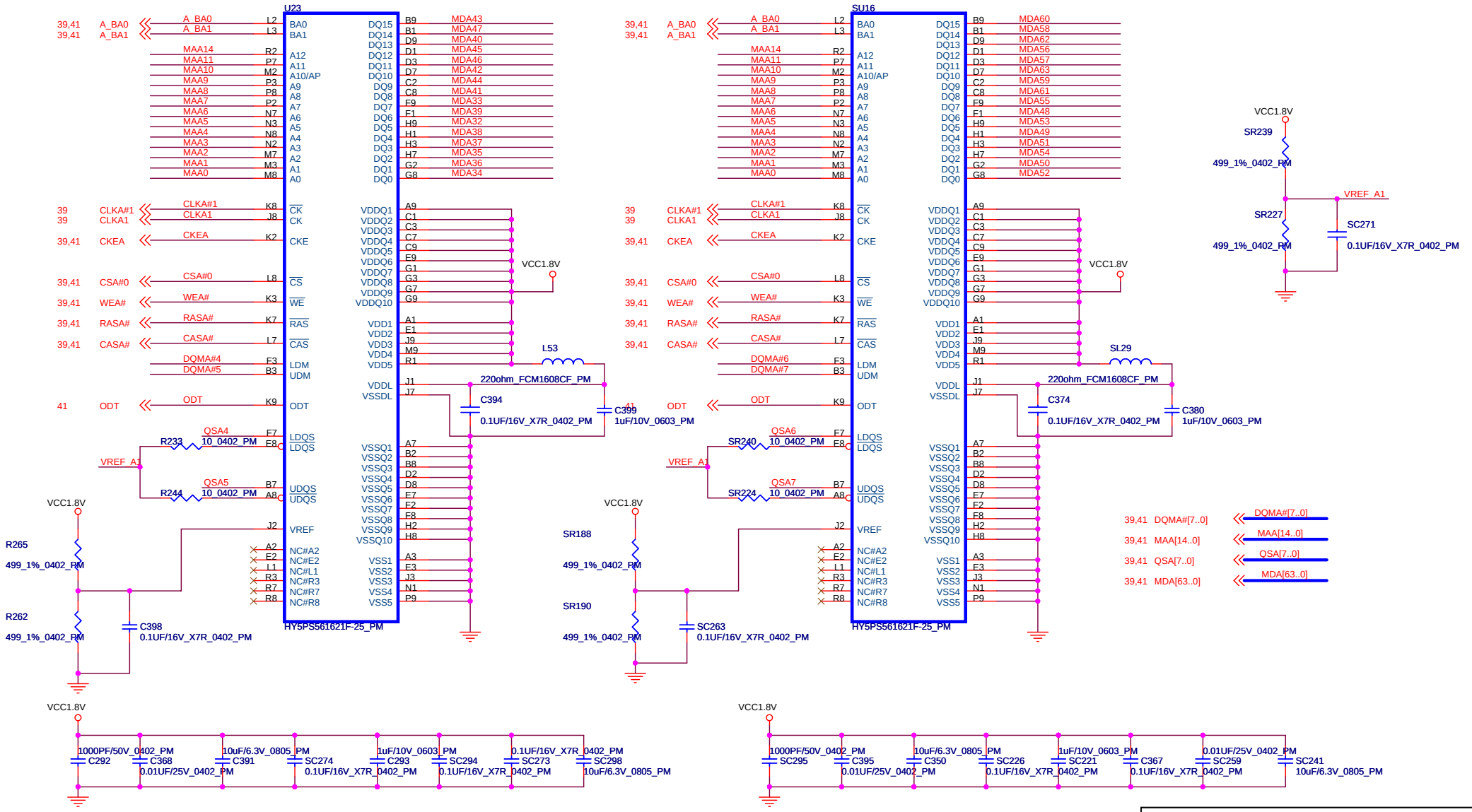
V1.0 Stage BOM Del Page 42 component FOR 32 bit



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Title	G420 DDR2 VRAM 16X16 B
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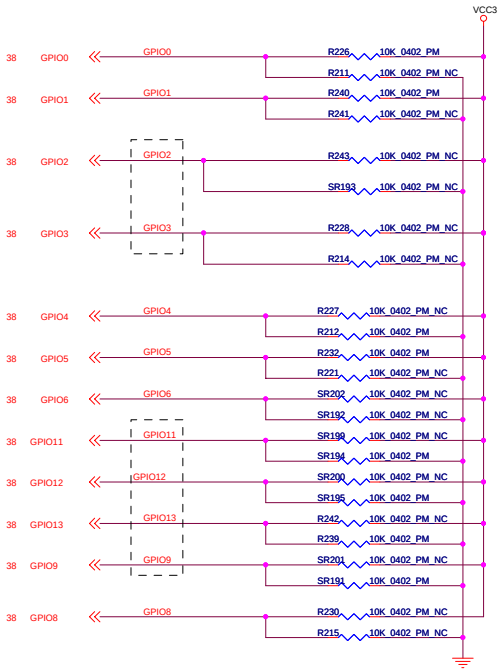
OPTION STRAPS



STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing 1.full Tx output swing	
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1.Tx de-emphasis enabled	
	GPIO(3:2)	RSVD	
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible (Debug_Access on M22T is GPIO8)	0
	GPIO5	RSVD	
	GPIO6	RSVD	
Force_Compliance	GPIO8	Force chip to get to compliance state quickly for Tester purposes	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port deviced present. 1-No slave VIP port devices reporting presence during reset	No default
	H2SYNC, V2SYNC, GENERICC	RSVD	
	VSYNC	RSVD	
	HSYNC	RSVD	
	PCIE_TEST	RSVD	

MULTIFUNC(1:0)	LCDDATA(17:16)	Multi-function device select **00 - single function device.** 01 - two function device. No AGP in either function 10 - two function device. AGP only in function 0 11 - two function device. AGP in both functions If BUSCFG pin based straps are set to PCI, then AGP will not be enabled in any function.	00
VIP_DEVICE	LCDDATA(20)	Indicates if any slave VIP host devices drove this low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	0
DWNGRD	LCDDATA(21)	0 - Device remain a workstation grade part. 1 - Part is downgraded to a Normal part	0 (internal pull-down)

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Title: G420 OPTION STRAPS

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420 M/B V.A initial release-05/10/21

420 M/B V.C initial release-06/02/20

P.22 CN2 PIN SWAP

420 M/B V.1.0 initial release-06/04/03

420 M/B V2.0 MODIFY PLEAST RESET PIN BUG

420 M/B V3.0 MODIFY GLAN

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Title: G420 HISTORY

Size	Document Number	Rev
Custom	420 -1-4-01	3.0

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