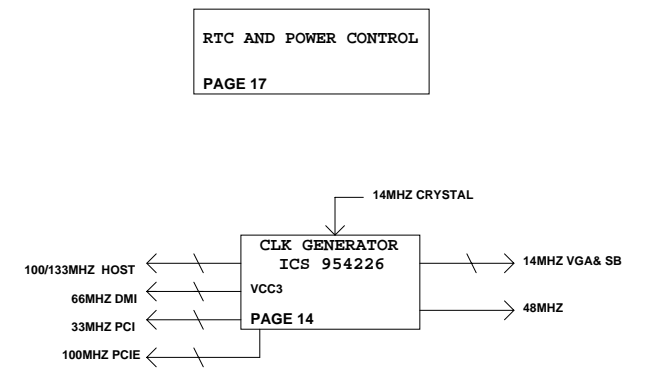
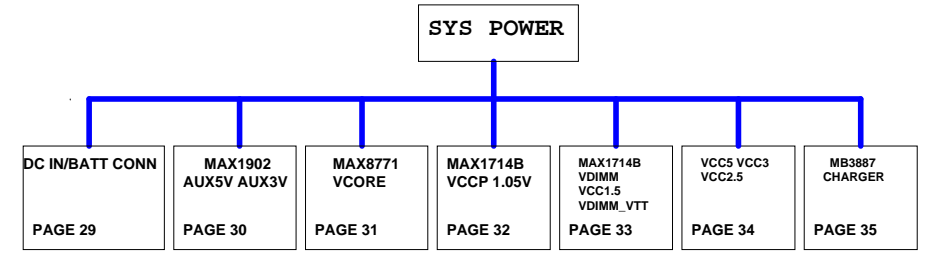
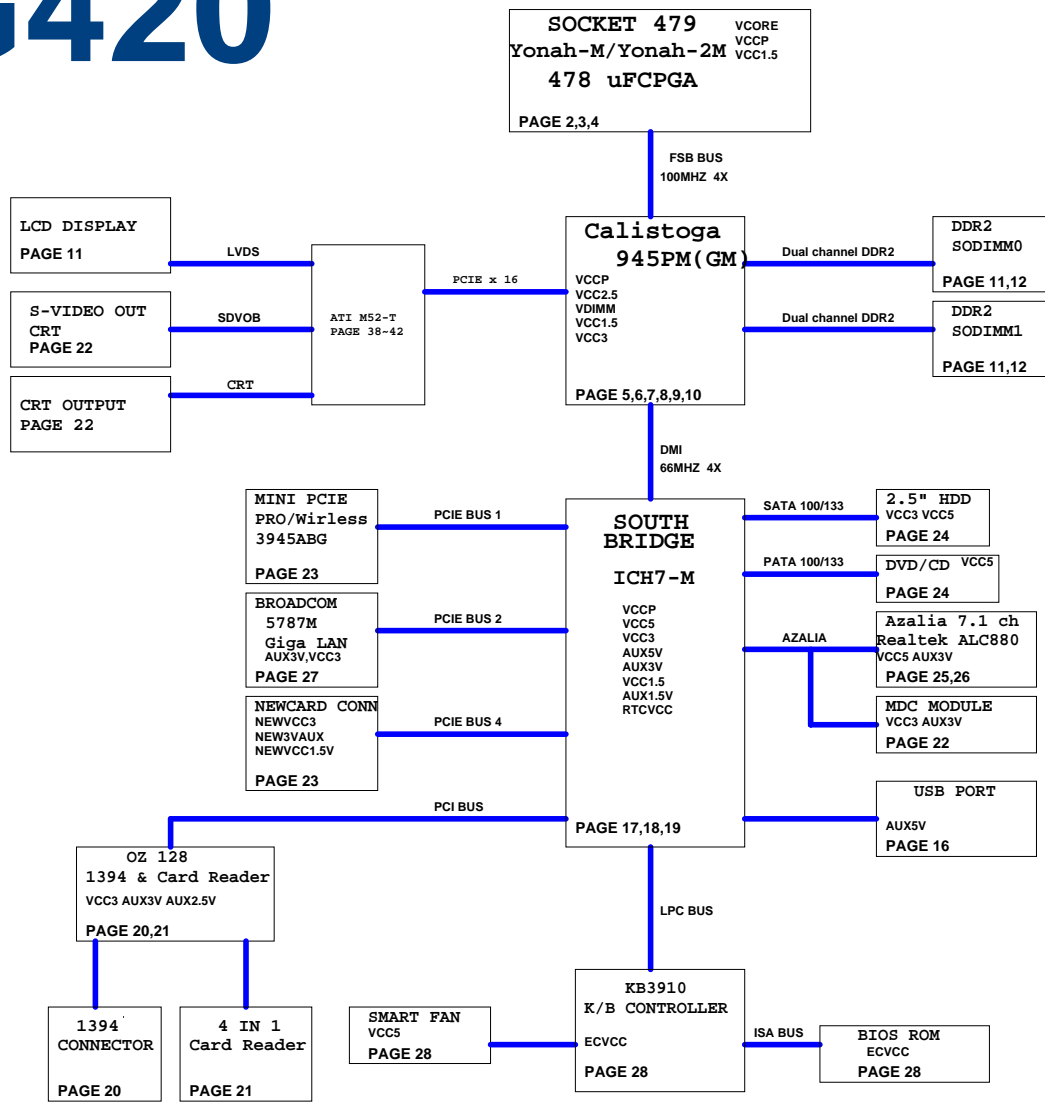


G420



POWER SEQUENCE BLOCK DIAGRAM
PAGE 36

HISTORY
PAGE 37

PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
REV	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0
DATE	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03
PAGE	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36
REV	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0
DATE	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03
PAGE	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54
REV	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0										
DATE	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03	06/08/03										

PCB P/N:15-F73-013000

P. Leader
Simon

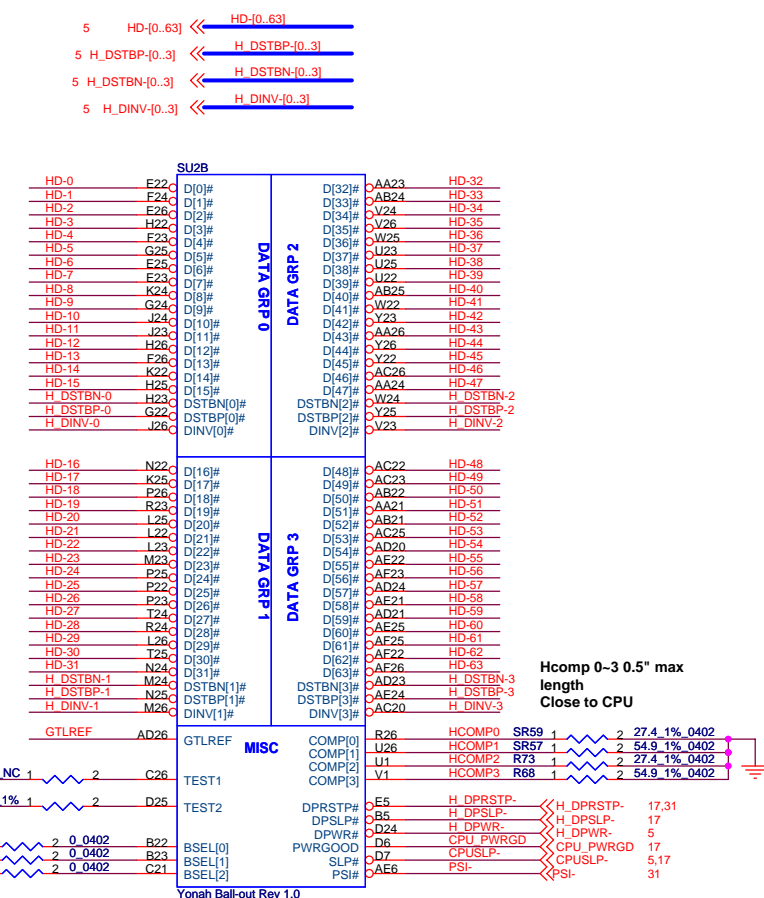
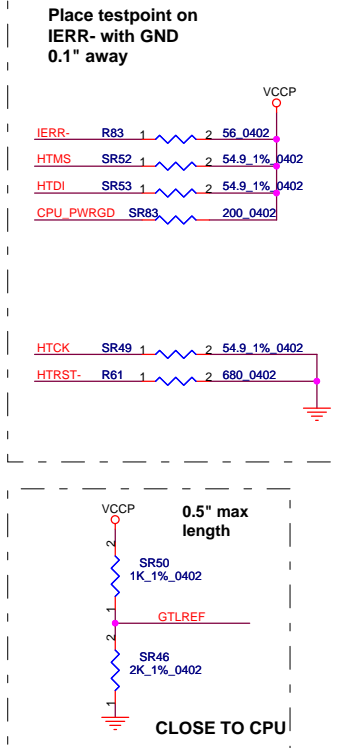
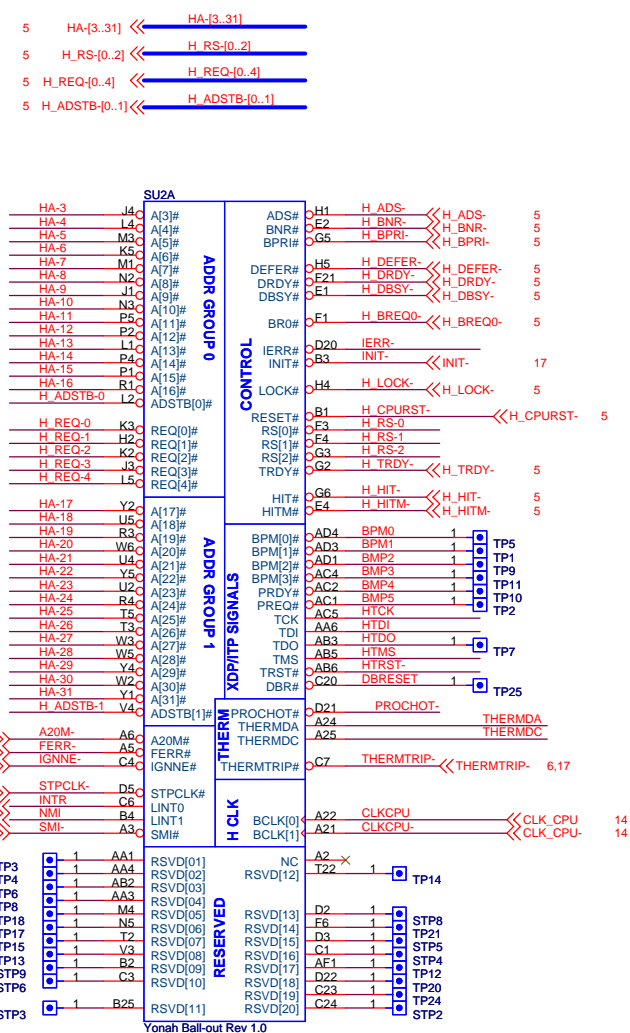
Approved by	Checked by	Designed by

Elitegroup Computer Systems

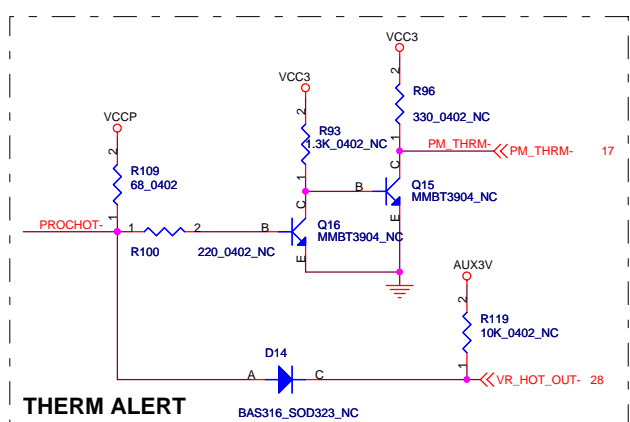
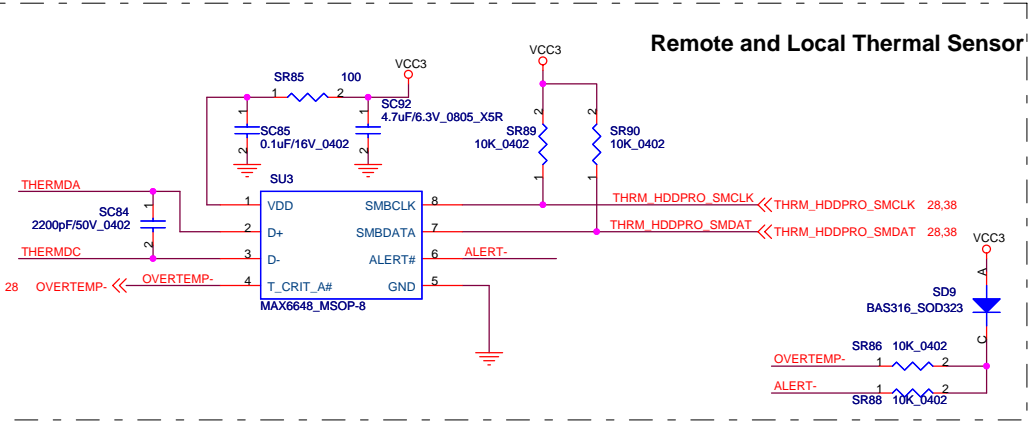
File: **G420 BLOCK DIAGRAM**

Size: A2 Document Number: 420-1-4-01 Row: 2.0

Date: Monday, August 21, 2006 Sheet: 1 of 44



R112 51 ohm:
Intel has determined that Test2 pin needs to be populated with a 51 ohm +/-5% resistor in order for Yonah B-0 silicon to boot due to issue in the reset sequence needed for the processor.



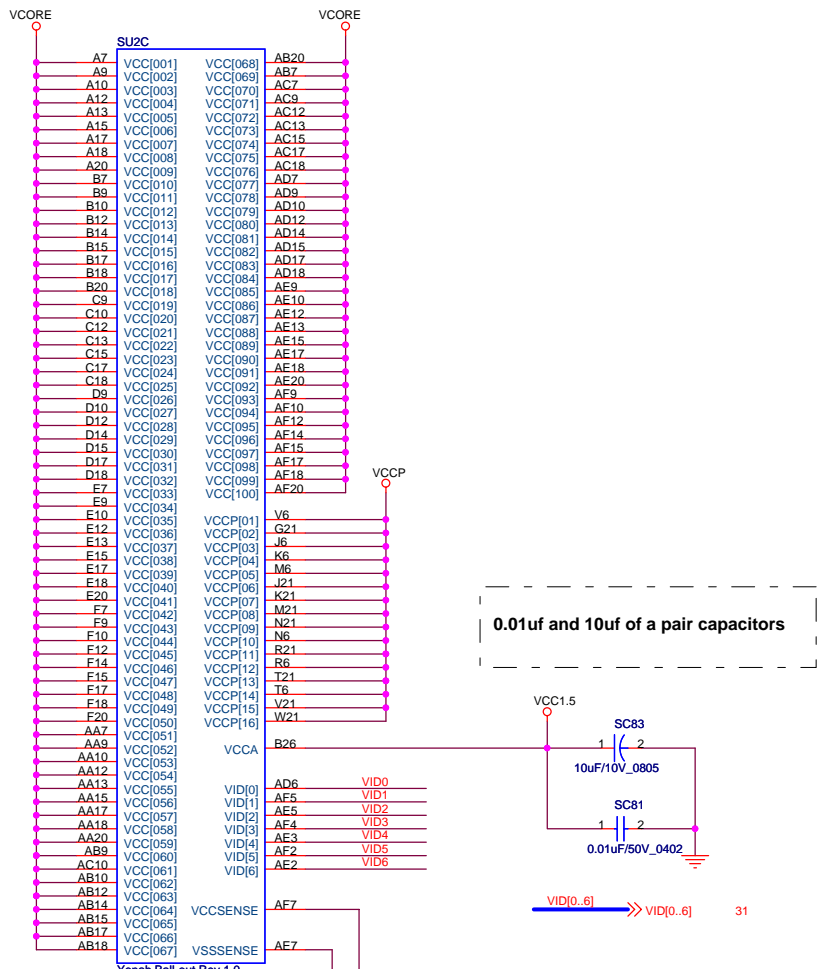
BSEL[0]	BSEL[1]	BSEL[2]	BCLK frequency
L	L	L	RESERVED
H	L	L	133MHZ
L	H	L	RESERVED
H	H	L	166MHZ

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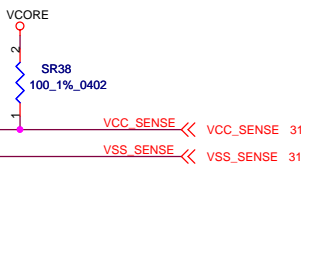
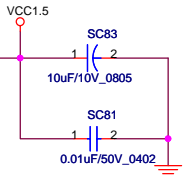
Title: **G420 Yonah-1**

Size A3 Document Number: **420 -1-4-01** Rev 3.0

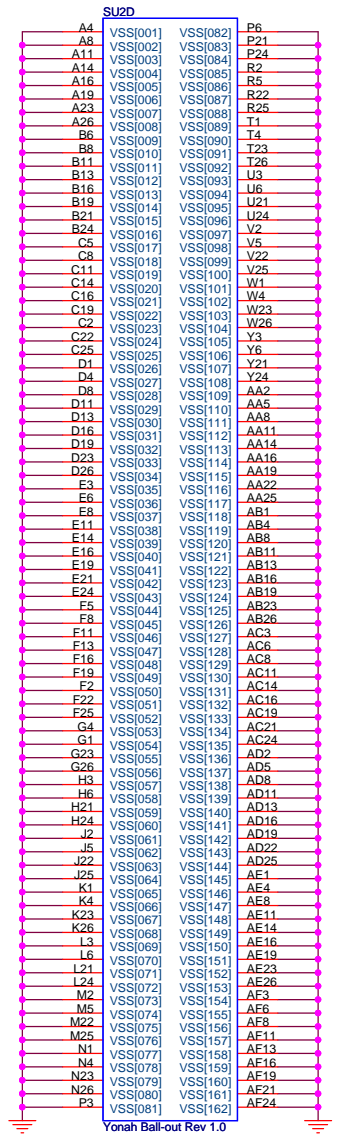
Date: Thursday, August 03, 2006 Sheet 2 of 44



0.01uf and 10uf of a pair capacitors



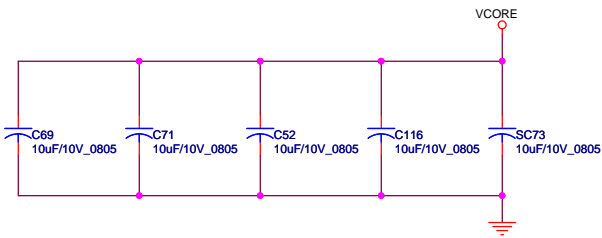
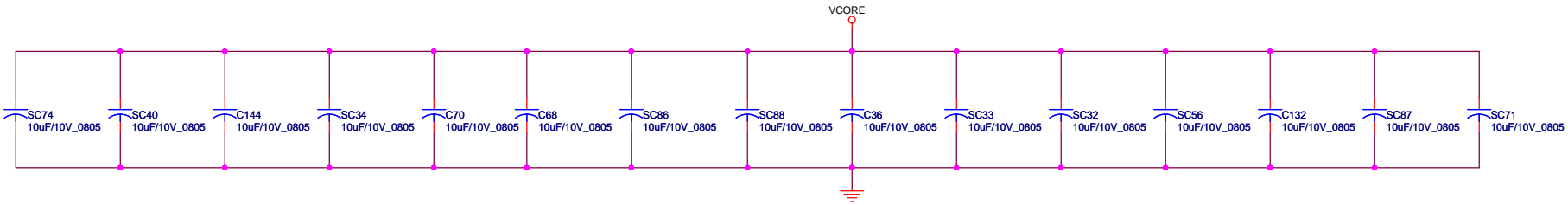
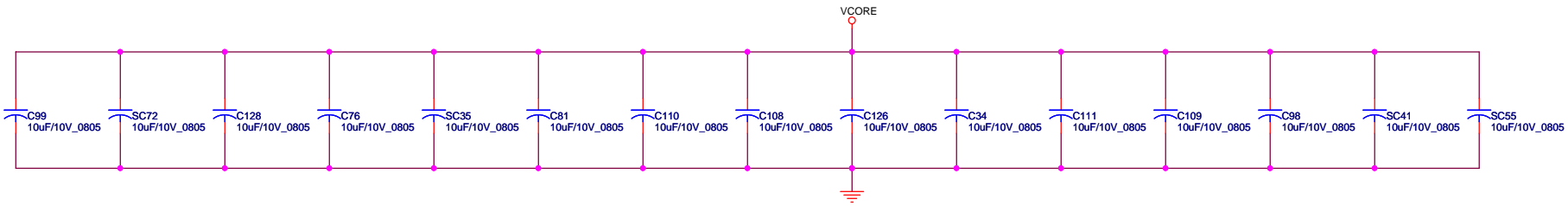
Layout Note:
 Route VCC_SENSE and VSS_SENSE trace at 27.4 ohm with 50 mil spacing.
 Place PU and PD within 1 inch of CPU.



ECS Elitegroup Computer Systems

Title: **G420 Yonah-2**

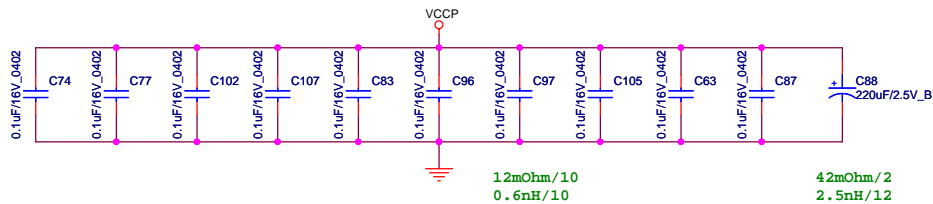
Size A3	Document Number 420 -1-4-01	Rev 3.0
Date: Thursday, August 03, 2006	Sheet 3 of 44	

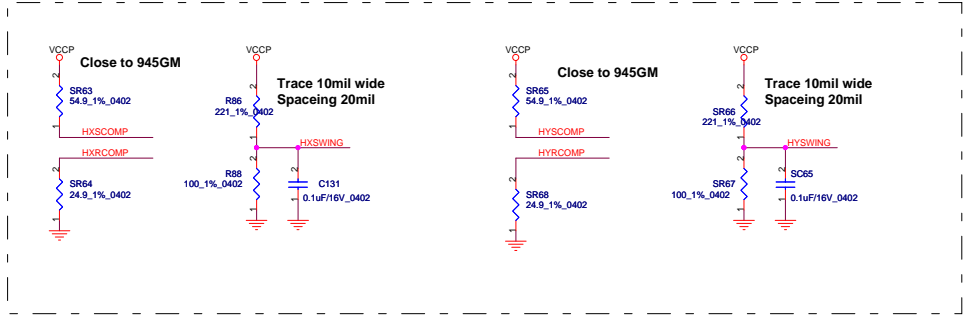
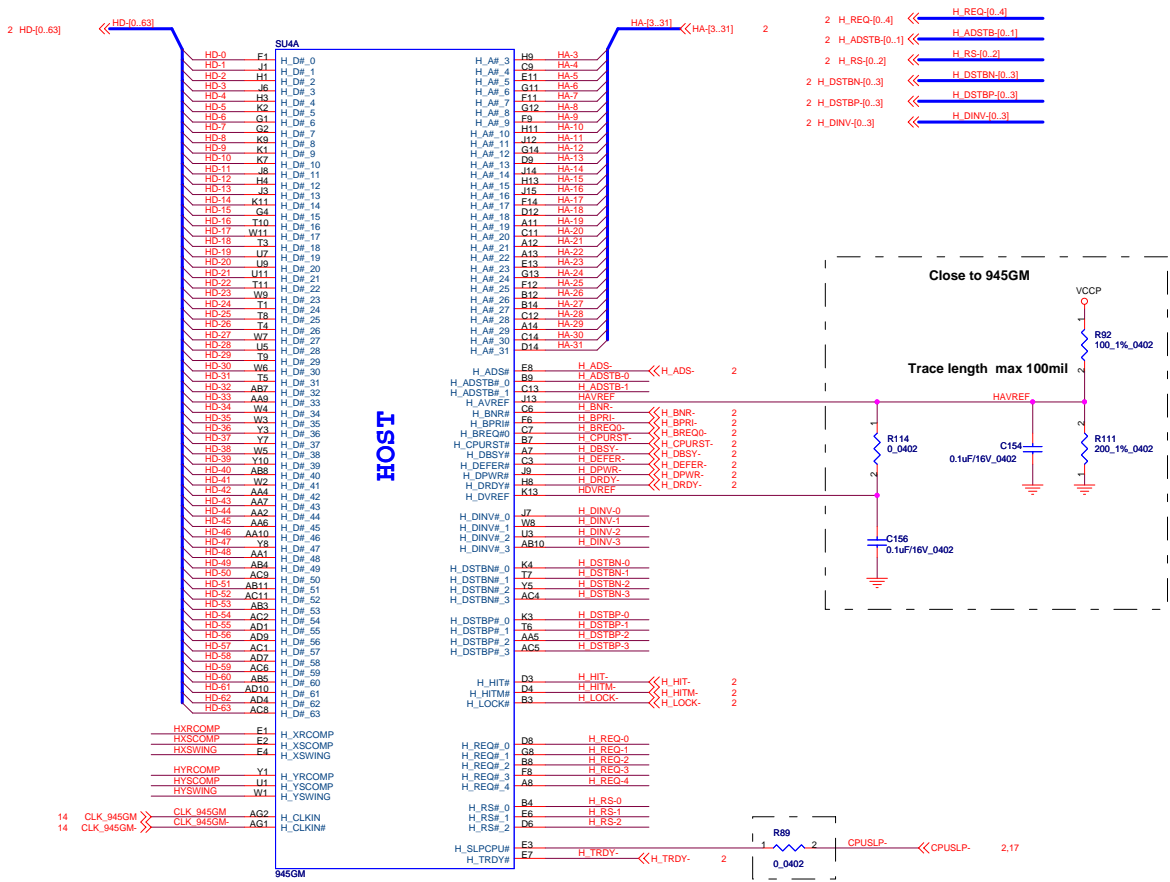


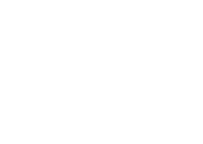
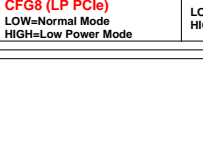
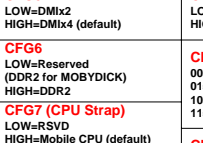
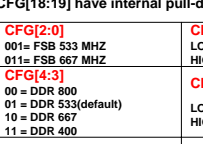
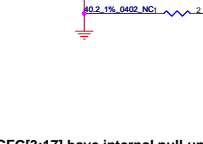
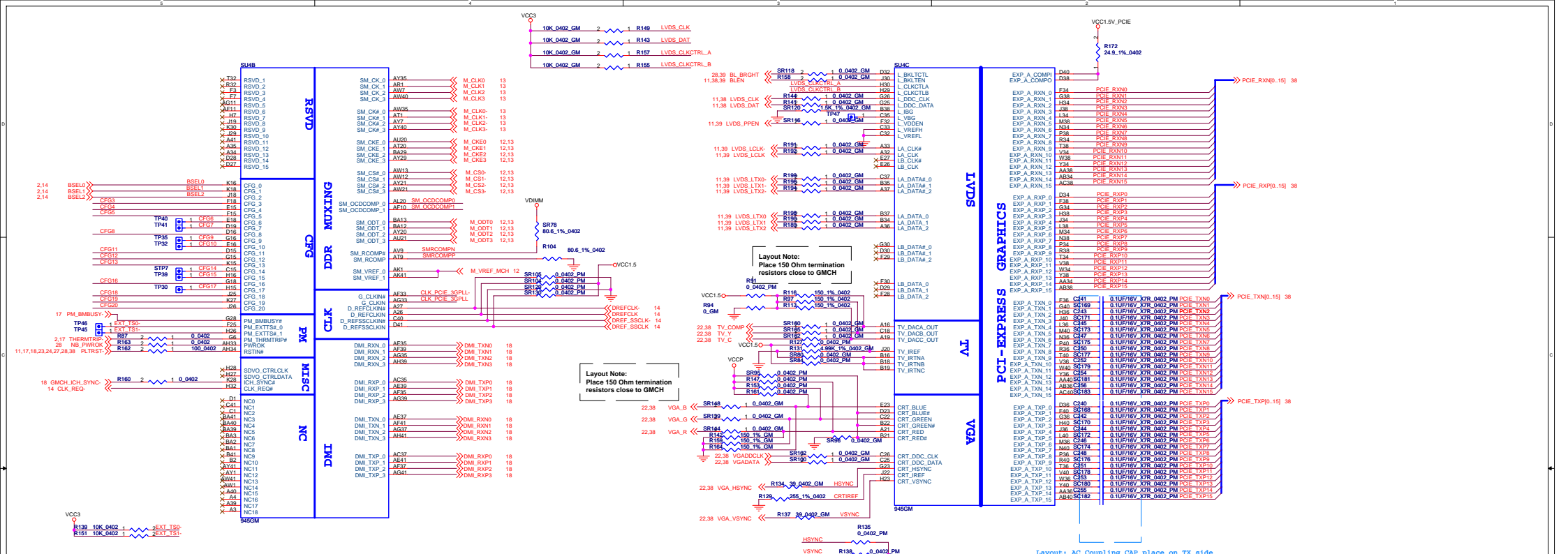
VCORE Bypass: Close to CPU Socket

5mOhm/35
0.6nH/35

VCCP Bypass: Close to CPU Socket

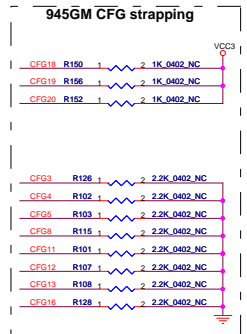




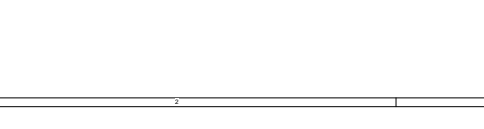
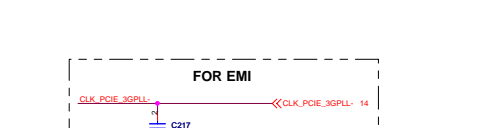


CFG[3:17] have internal pull-ups
CFG[18:19] have internal pull-downs

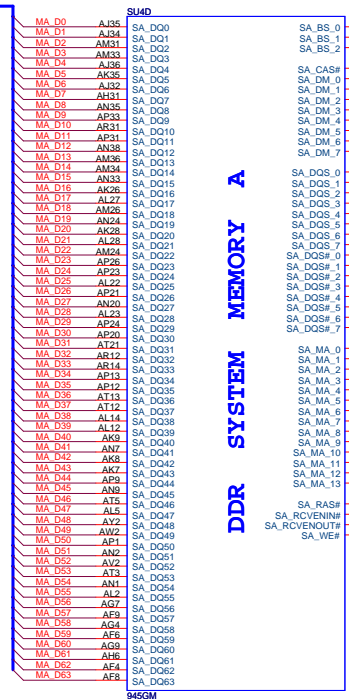
<p>CFG[2:0] 001= FSB 533 MHZ 011= FSB 667 MHZ</p> <p>CFG[4:3] 00 = DDR 800 01 = DDR 533(default) 10 = DDR 667 11 = DDR 400</p> <p>CFG5 LOW=DMIX2 HIGH=DMIX4 (default)</p> <p>CFG6 LOW=Reserved (DDR2 for MOBVDICK) HIGH=DDR2</p> <p>CFG7 (CPU Strap) LOW=RSVD HIGH=Mobile CPU (default)</p> <p>CFG8 (LP PCIe) LOW=Normal Mode HIGH=Low Power Mode</p>	<p>CFG9(PCIE Graphics Lane) LOW= Reversal Lane HIGH=Normal Operation (default)</p> <p>CFG10 (HOST PLL VCC SELET) LOW=Reserved HIGH=MOBILITY</p> <p>CFG11 (PSB 4X CLK ENABLE) LOW= 4X ENABLED HIGH=8X ENABLED</p> <p>CFG[13:12] 00=Partial Clock Gating Disable 01=XOR Mode Enable 10=All-Z Mode Enable 11=Normal Operation (Default)</p> <p>CFG14 DF STRAP ENABLE LOW=DF STRAP ENABLE HIGH=Normal Operation</p>	<p>CFG15 (ICH RESET DISABLE) LOW= ICH RESET DISABLE HIGH=Normal Operation</p> <p>CFG16 (FSB Dynamic ODT) LOW=Dynamic ODT Disabled HIGH=Dynamic ODT Enabled (default)</p> <p>CFG17(Global Rcomp Disable) LOW=All Rcomp Disable HIGH=Normal Operation</p> <p>CFG18 (VCC SELECT) LOW=1.05V (default) HIGH=1.5V</p> <p>CFG19 (DMI LANE RESERVED) LOW=Normal HIGH=LANES REVERSED (default)</p>	<p>CFG20 (PCIe Backward Interoperability mode) LOW=only SDVO or PCIE x1 is operational (defaults) HIGH=SDVO and PCIE x1 are operating simultaneously via the PEG port</p>
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Layout Note:
Place 150 Ohm termination resistors close to GMCH

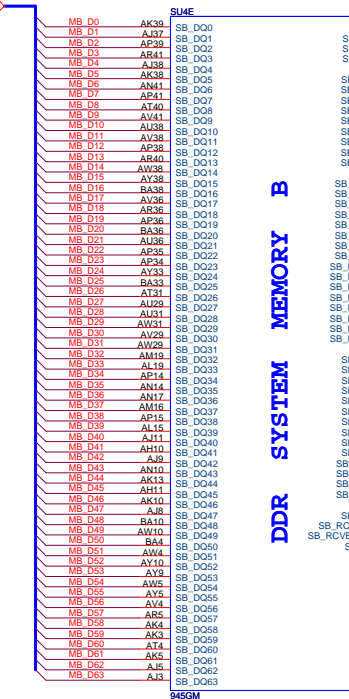


13 MA_D[0..63] >>

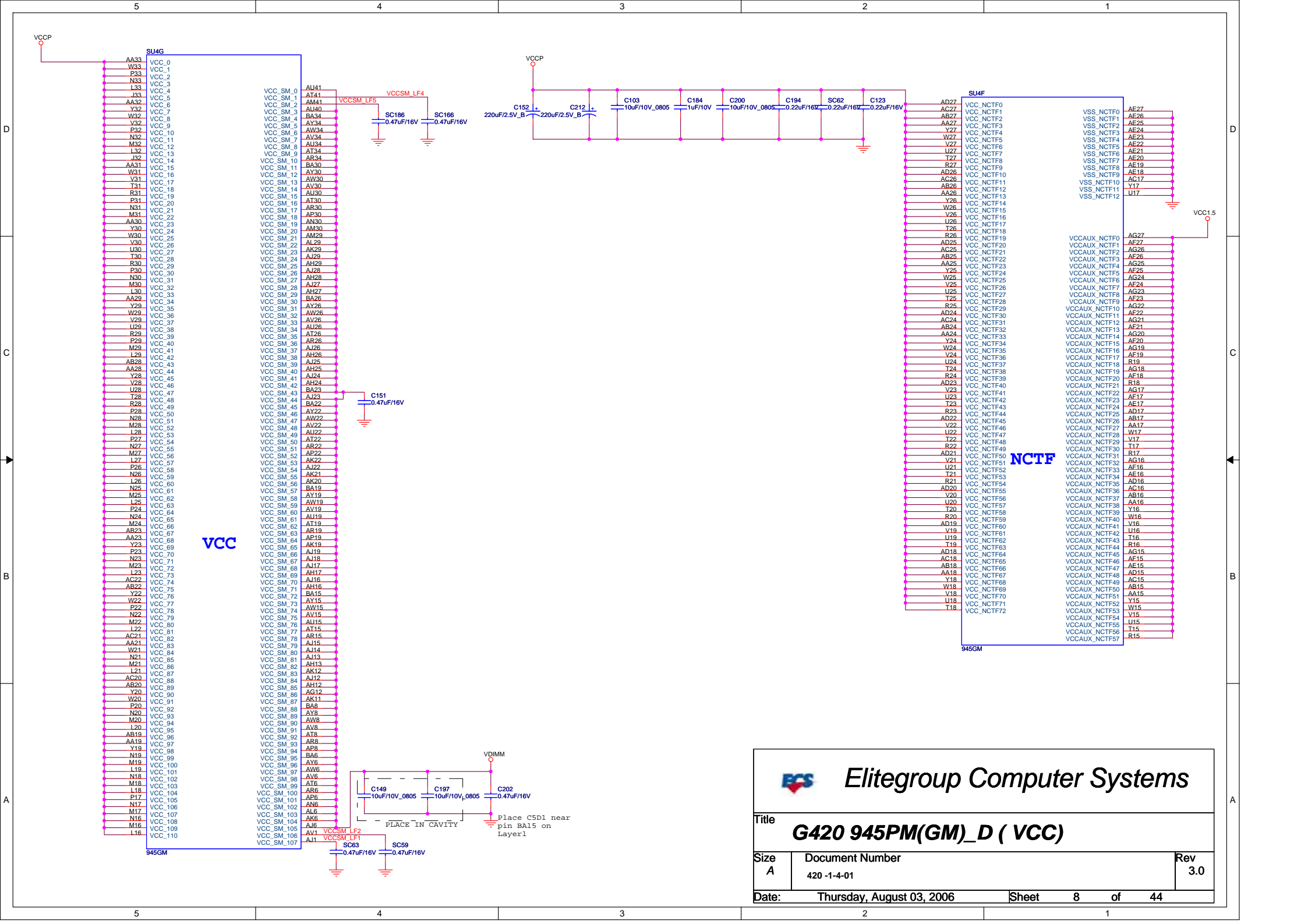



945GM

13 MB_D[0..63] >>



945GM

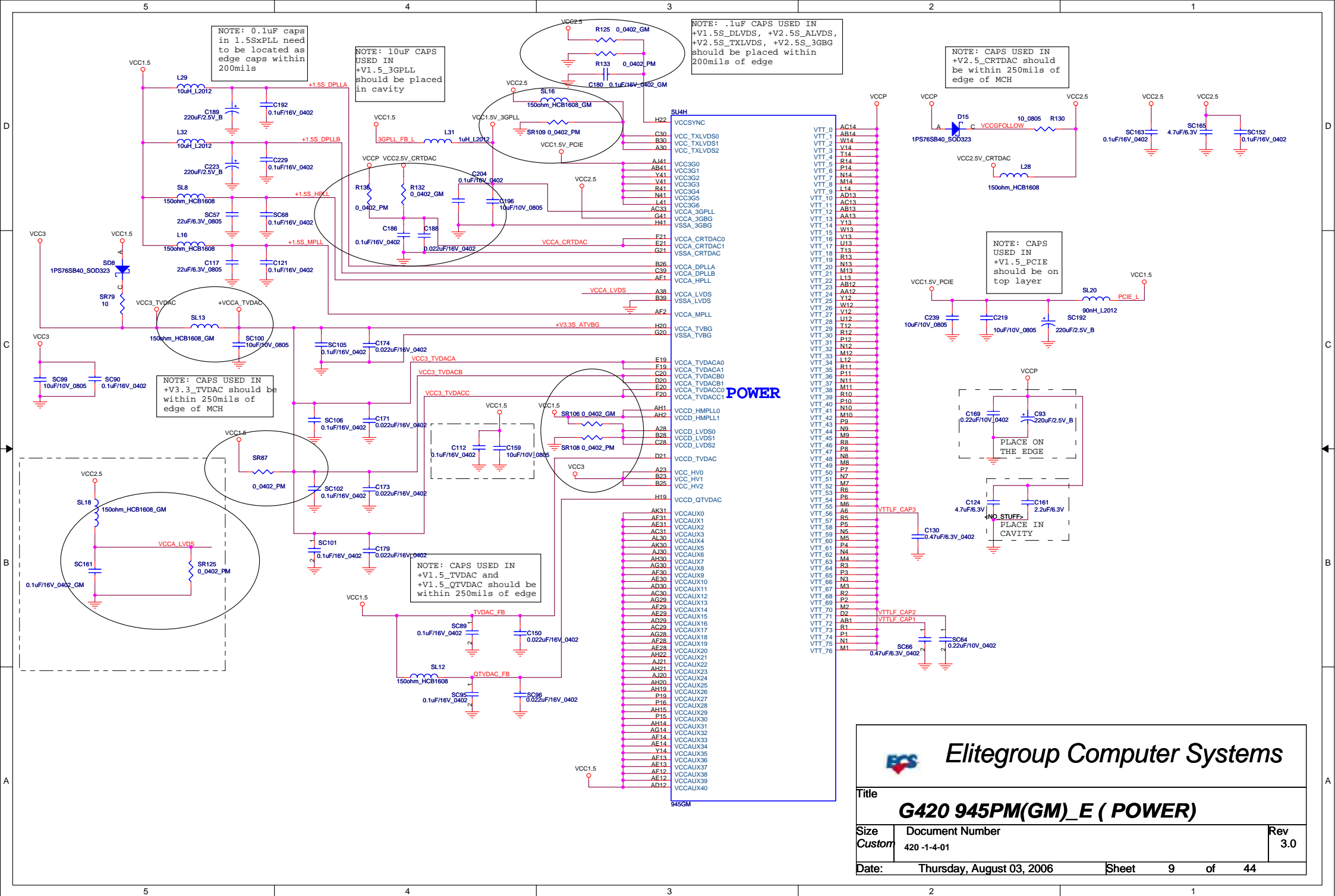



Elitegroup Computer Systems

Title: **G420 945PM(GM)_D (VCC)**

Size A	Document Number 420 -1-4-01	Rev 3.0
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Date: **Thursday, August 03, 2006** Sheet **8** of **44**



NOTE: 0.1uF caps in 1.5SxPLL need to be located as edge caps within 200mils

NOTE: 10uF CAPS USED IN +V1.5_3GPLL should be placed in cavity

NOTE: .1uF CAPS USED IN +V1.5S_DLVDs, +V2.5S_ALVDs, +V2.5S_TXLVDs, +V2.5S_3GBG should be placed within 200mils of edge

NOTE: CAPS USED IN +V2.5_CRTDAC should be within 250mils of edge of MCH

NOTE: CAPS USED IN +V3.3_TVDC should be within 250mils of edge of MCH

NOTE: CAPS USED IN +V1.5_TVDC and +V1.5_QTVDC should be within 250mils of edge

NOTE: CAPS USED IN +V1.5_PCIE should be on top layer

PLACE ON THE EDGE

NO STUFF PLACE IN CAVITY

POWER

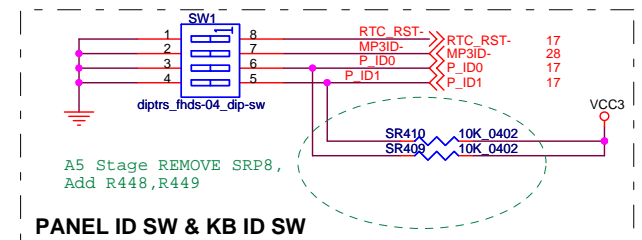
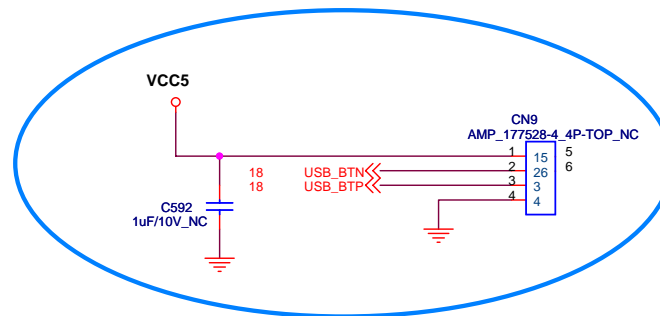
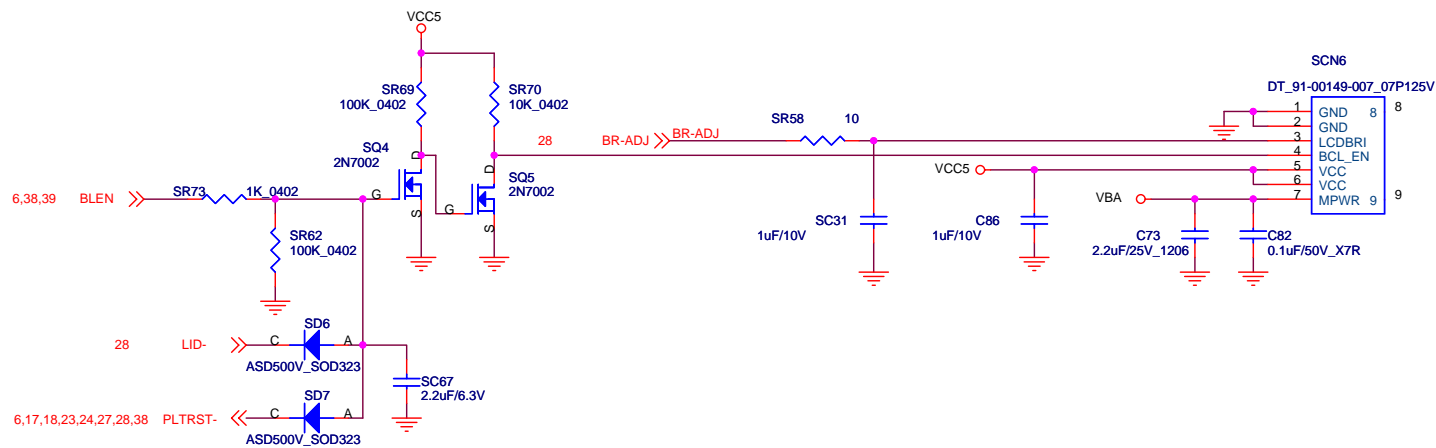
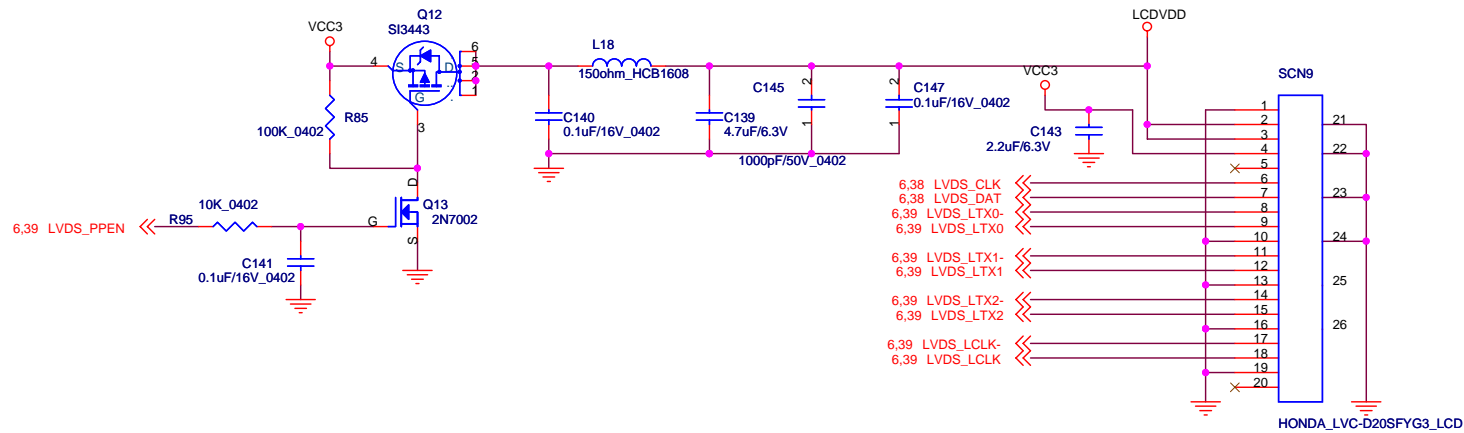


Elitegroup Computer Systems

Title		
G420 945PM(GM)_E (POWER)		
Size	Document Number	Rev
Custom	420-1-4-01	3.0
Date:	Thursday, August 03, 2006	Sheet 9 of 44

SI44		AK34	
AC41	VSS_0	VSS_97	AK34
AA41	VSS_1	VSS_98	AF34
WA41	VSS_2	VSS_99	AE34
T41	VSS_3	VSS_100	AC34
P41	VSS_4	VSS_101	C41
M41	VSS_5	VSS_102	AW33
K41	VSS_6	VSS_103	AV33
F41	VSS_7	VSS_104	AR33
AV40	VSS_8	VSS_105	AE33
AP40	VSS_9	VSS_106	AB33
AN40	VSS_10	VSS_107	T33
AK40	VSS_11	VSS_108	V33
A40	VSS_12	VSS_109	T33
AH40	VSS_13	VSS_110	M33
AG40	VSS_14	VSS_111	H33
AE40	VSS_15	VSS_112	R33
E40	VSS_16	VSS_113	D33
AY39	VSS_17	VSS_114	F33
AW39	VSS_18	VSS_115	G33
AV39	VSS_19	VSS_116	D33
AR39	VSS_20	VSS_117	AH32
AN39	VSS_21	VSS_118	AG32
A39	VSS_22	VSS_119	AF32
AC39	VSS_23	VSS_120	AE32
AB39	VSS_24	VSS_121	AC32
AA39	VSS_25	VSS_122	AB32
Y39	VSS_26	VSS_123	G32
W39	VSS_27	VSS_124	H21
V39	VSS_28	VSS_125	C21
U39	VSS_29	VSS_126	AV20
T39	VSS_30	VSS_127	AV31
R39	VSS_31	VSS_128	AN31
P39	VSS_32	VSS_129	AK31
N39	VSS_33	VSS_130	AG31
M39	VSS_34	VSS_131	AW31
L39	VSS_35	VSS_132	V31
J39	VSS_36	VSS_133	AB30
H39	VSS_37	VSS_134	E31
G39	VSS_38	VSS_135	AT29
F39	VSS_39	VSS_136	AN29
D39	VSS_40	VSS_137	AB29
AT38	VSS_41	VSS_138	T29
AM38	VSS_42	VSS_139	N29
AG38	VSS_43	VSS_140	K29
AE38	VSS_44	VSS_141	G29
E38	VSS_45	VSS_142	E29
C38	VSS_46	VSS_143	C29
AK37	VSS_47	VSS_144	B29
AH37	VSS_48	VSS_145	A29
AB37	VSS_49	VSS_146	BA28
AA37	VSS_50	VSS_147	AW28
Y37	VSS_51	VSS_148	AU28
W37	VSS_52	VSS_149	AP28
V37	VSS_53	VSS_150	AM28
U37	VSS_54	VSS_151	AD28
T37	VSS_55	VSS_152	AC28
R37	VSS_56	VSS_153	W28
P37	VSS_57	VSS_154	J28
N37	VSS_58	VSS_155	F28
M37	VSS_59	VSS_156	AP27
L37	VSS_60	VSS_157	AM27
J37	VSS_61	VSS_158	AK27
H37	VSS_62	VSS_159	J27
G37	VSS_63	VSS_160	G27
F37	VSS_64	VSS_161	F27
D37	VSS_65	VSS_162	C27
AY36	VSS_66	VSS_163	B27
AW36	VSS_67	VSS_164	AN26
AV36	VSS_68	VSS_165	M26
AR36	VSS_69	VSS_166	K26
AN36	VSS_70	VSS_167	F26
A36	VSS_71	VSS_168	D26
AC36	VSS_72	VSS_169	P26
AB36	VSS_73	VSS_170	K26
AA36	VSS_74	VSS_171	H26
Y36	VSS_75	VSS_172	E26
W36	VSS_76	VSS_173	D26
V36	VSS_77	VSS_174	A26
U36	VSS_78	VSS_175	BA24
T36	VSS_79	VSS_176	AD24
R36	VSS_80	VSS_177	AL24
P36	VSS_81	VSS_178	AW23
N36	VSS_82	VSS_179	
M36	VSS_83	VSS_180	
L36	VSS_84	VSS_181	
J36	VSS_85	VSS_182	
H36	VSS_86	VSS_183	
G36	VSS_87	VSS_184	
F36	VSS_88	VSS_185	
D36	VSS_89	VSS_186	
AN34	VSS_90	VSS_187	
	VSS_91	VSS_188	
	VSS_92	VSS_189	
	VSS_93	VSS_190	
	VSS_94	VSS_191	
	VSS_95	VSS_192	
	VSS_96	VSS_193	
	VSS_97	VSS_194	
	VSS_98	VSS_195	

SI44		AK34	
AT23	VSS_180	VSS_273	J11
AM23	VSS_181	VSS_274	D11
AK23	VSS_182	VSS_275	B11
AC23	VSS_183	VSS_276	AV10
W23	VSS_184	VSS_277	AP10
K23	VSS_185	VSS_278	AL10
J23	VSS_186	VSS_279	AG10
F23	VSS_187	VSS_280	AG10
C23	VSS_188	VSS_281	AC10
AA22	VSS_189	VSS_282	AW10
K22	VSS_190	VSS_283	L10
G22	VSS_191	VSS_284	AW9
F22	VSS_192	VSS_285	AN9
D22	VSS_193	VSS_286	AR9
A22	VSS_194	VSS_287	AB9
PA21	VSS_195	VSS_288	AN9
AV21	VSS_196	VSS_289	Y9
AR21	VSS_197	VSS_290	G9
AN21	VSS_198	VSS_291	AS
AL21	VSS_199	VSS_292	E9
Y21	VSS_200	VSS_293	AG8
K21	VSS_201	VSS_294	AR8
H21	VSS_202	VSS_295	AD8
C21	VSS_203	VSS_296	U8
AV20	VSS_204	VSS_297	AS
AR20	VSS_205	VSS_298	CS
AM20	VSS_206	VSS_299	BA7
AK20	VSS_207	VSS_300	CA
AC20	VSS_208	VSS_301	AV7
W20	VSS_209	VSS_302	AF7
K20	VSS_210	VSS_303	AL7
J20	VSS_211	VSS_304	AJ7
F20	VSS_212	VSS_305	AH7
C20	VSS_213	VSS_306	AF7
AA20	VSS_214	VSS_307	AC7
K19	VSS_215	VSS_308	R7
AN19	VSS_216	VSS_309	G7
AK19	VSS_217	VSS_310	DT
AC19	VSS_218	VSS_311	AG6
W19	VSS_219	VSS_312	AD6
AR19	VSS_220	VSS_313	Y6
AM19	VSS_221	VSS_314	NE
AK19	VSS_222	VSS_315	U6
AC19	VSS_223	VSS_316	KE
W19	VSS_224	VSS_317	H6
AR19	VSS_225	VSS_318	B6
AM19	VSS_226	VSS_319	AV5
AK19	VSS_227	VSS_320	AF5
AC19	VSS_228	VSS_321	AD5
W19	VSS_229	VSS_322	AY4
AR19	VSS_230	VSS_323	AR4
AM19	VSS_231	VSS_324	AP4
AK19	VSS_232	VSS_325	AL4
AC19	VSS_233	VSS_326	AL4
W19	VSS_234	VSS_327	A4
AR19	VSS_235	VSS_328	Y4
AM19	VSS_236	VSS_329	U4
AK19	VSS_237	VSS_330	R4
AC19	VSS_238	VSS_331	J4
W19	VSS_239	VSS_332	CA
AR19	VSS_240	VSS_333	F4
AM19	VSS_241	VSS_334	AV3
AK19	VSS_242	VSS_335	AW3
AC19	VSS_243	VSS_336	AL3
W19	VSS_244	VSS_337	AG3
AR19	VSS_245	VSS_338	AH3
AM19	VSS_246	VSS_339	AF3
AK19	VSS_247	VSS_340	AD3
AC19	VSS_248	VSS_341	AC3
W19	VSS_249	VSS_342	AA3
AR19	VSS_250	VSS_343	G3
AM19	VSS_251	VSS_344	AT2
AK19	VSS_252	VSS_345	AR2
AC19	VSS_253	VSS_346	AP2
W19	VSS_254	VSS_347	AN2
AR19	VSS_255	VSS_348	AJ2
AM19	VSS_256	VSS_349	AD2
AK19	VSS_257	VSS_350	AB2
AC19	VSS_258	VSS_351	Y2
W19	VSS_259	VSS_352	U2
AR19	VSS_260	VSS_353	L2
AM19	VSS_261	VSS_354	T2
AK19	VSS_262	VSS_355	N2
AC19	VSS_263	VSS_356	J2
W19	VSS_264	VSS_357	H2
AR19	VSS_265	VSS_358	F2
AM19	VSS_266	VSS_359	CS
AK19	VSS_267	VSS_360	AL1
AC19	VSS_268		
W19	VSS_269		
AR19	VSS_270		
AM19	VSS_271		
AK19	VSS_272		



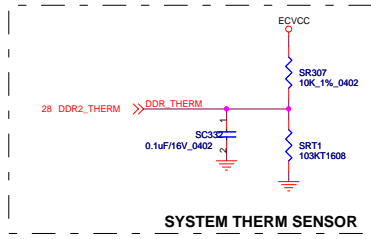
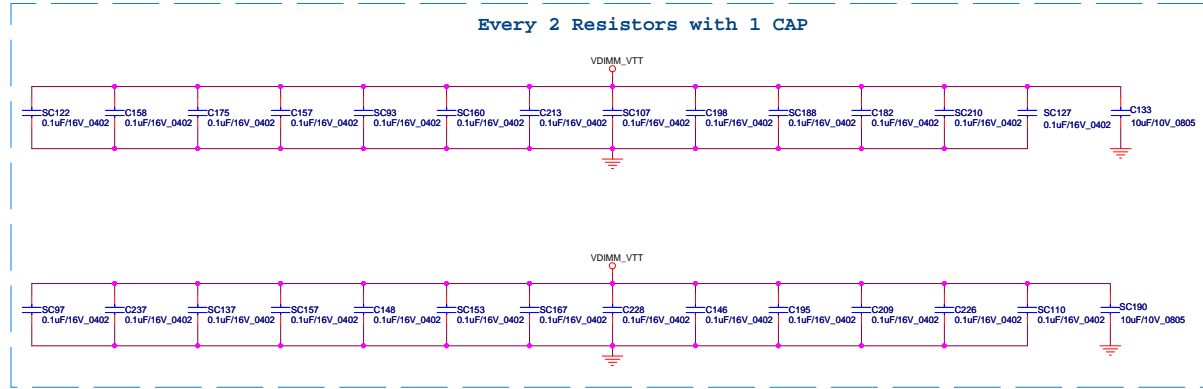
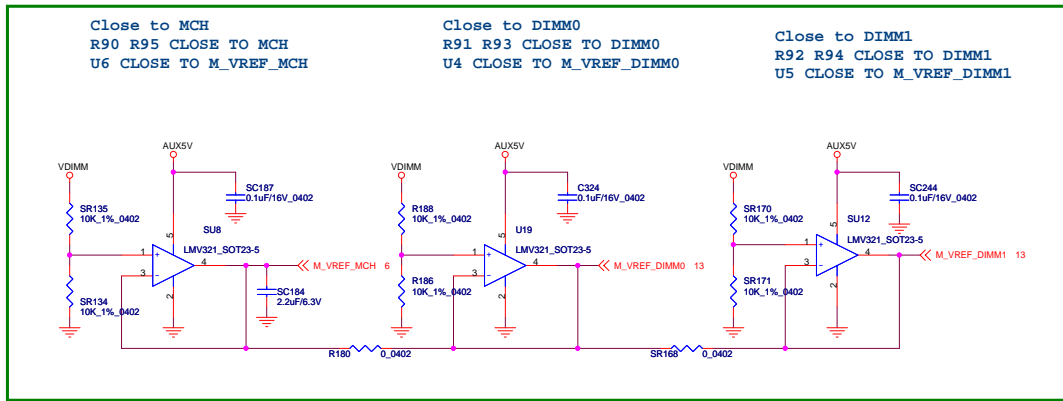
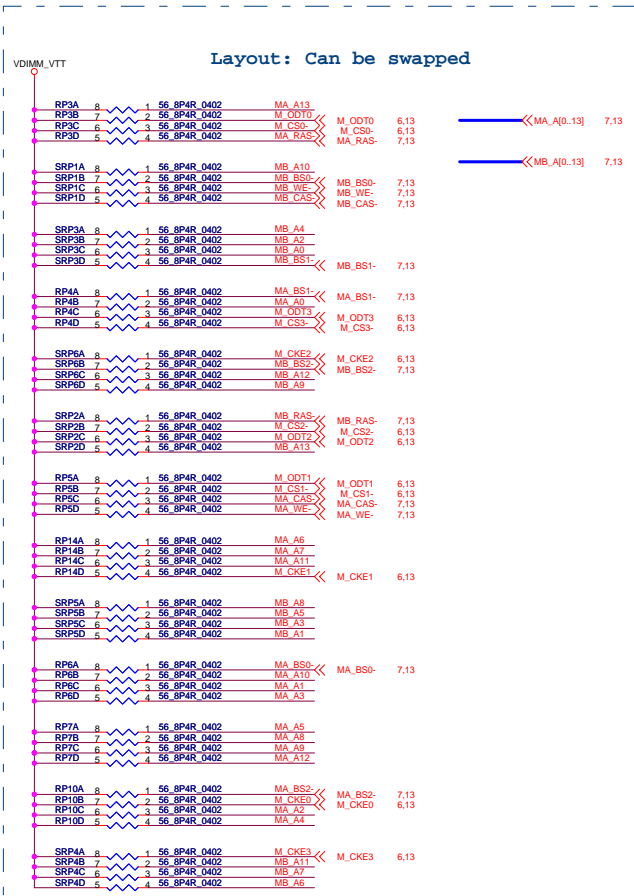
V1.0 Stage BOM Del CN9,C592

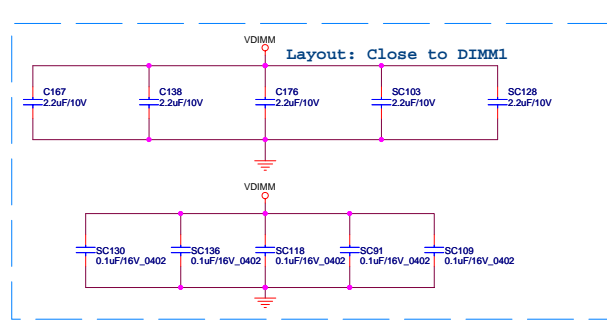
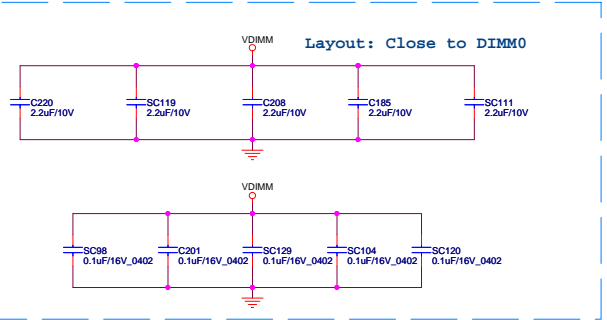
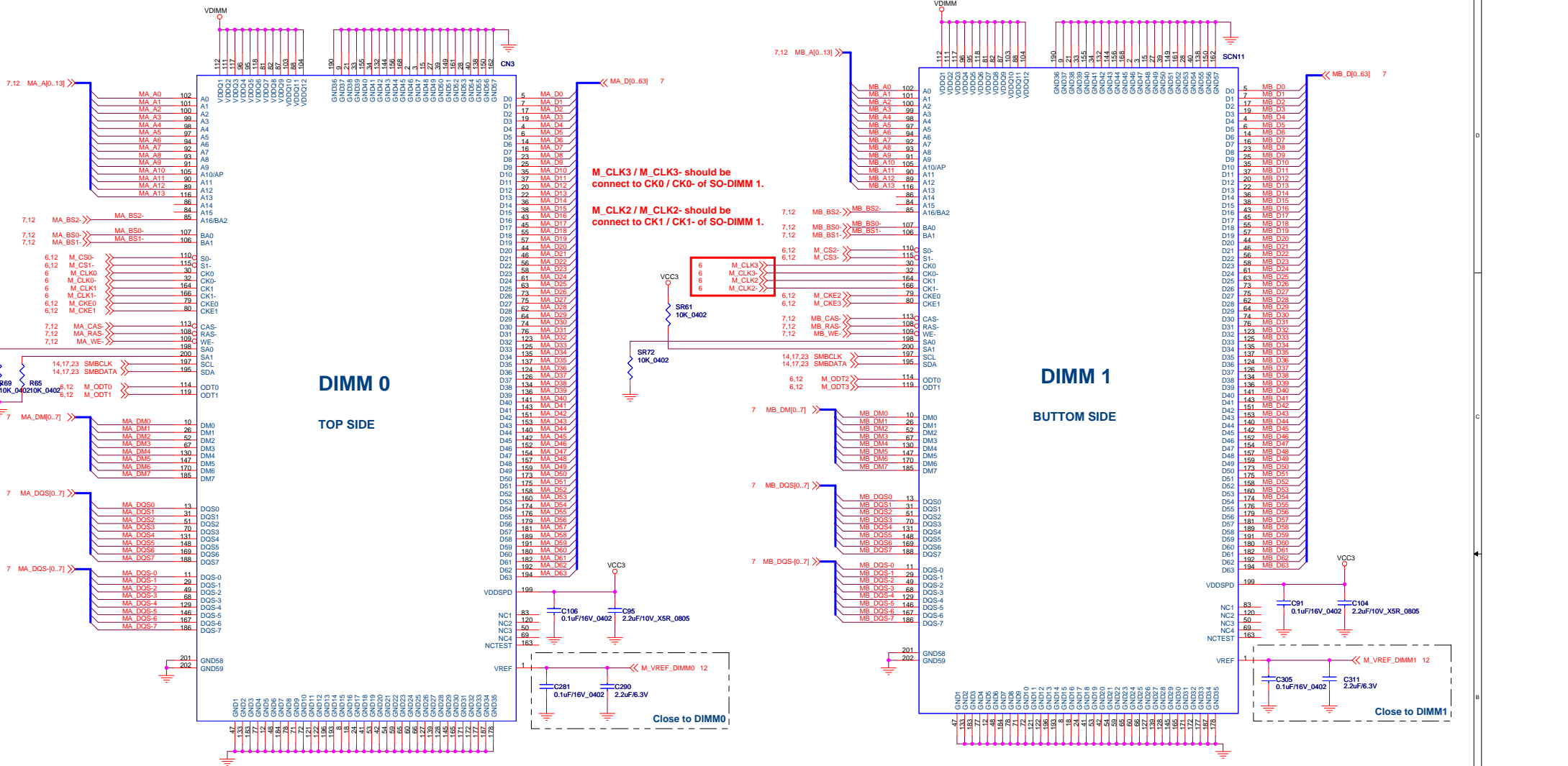
ECS Elitegroup Computer Systems

Title: **G420 LVDS**

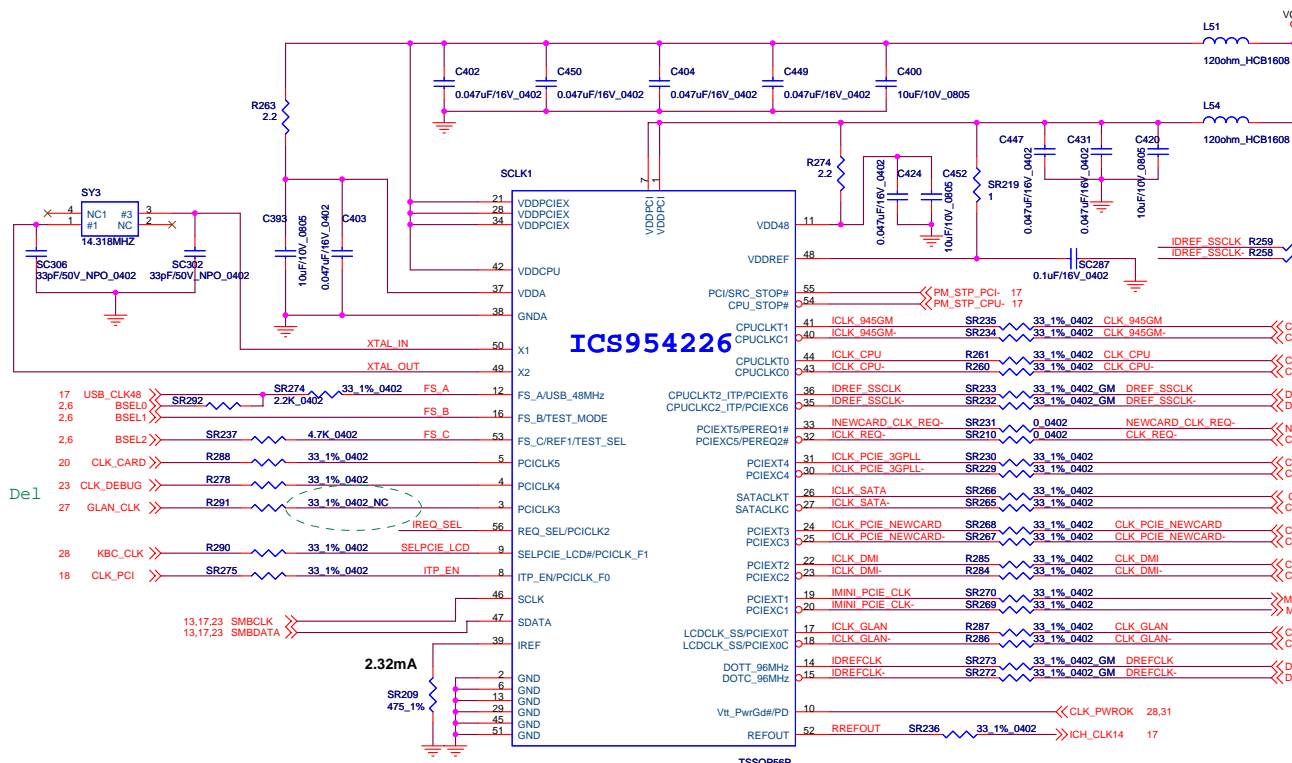
Size: Custom Document Number: 420 -1-4-01 Rev: 3.0

Date: Thursday, August 03, 2006 Sheet: 11 of 44



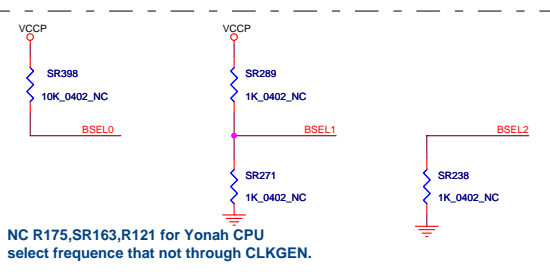
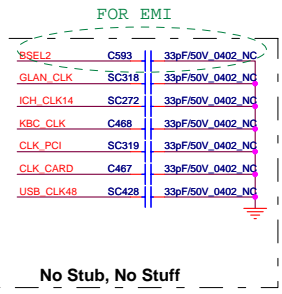
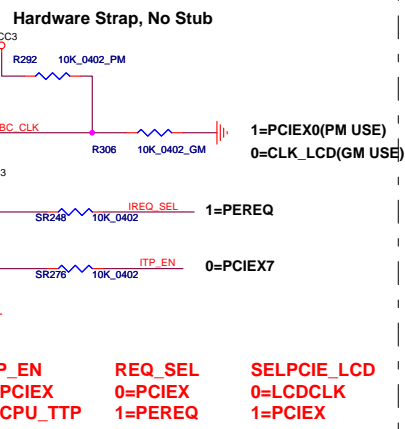
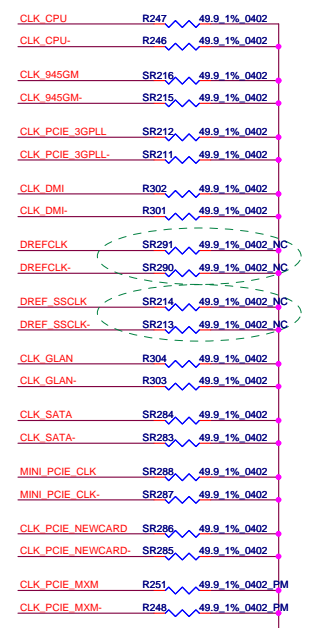


A5 Stage Del
R291

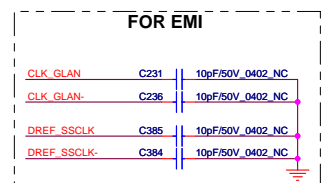


A5 Stage Del
SR291, SR290 SR214, SR213

Source Shunt Termination: No Stub



NC R175,SR163,R121 for Yonah CPU
select frequency that not through CLKGEN.



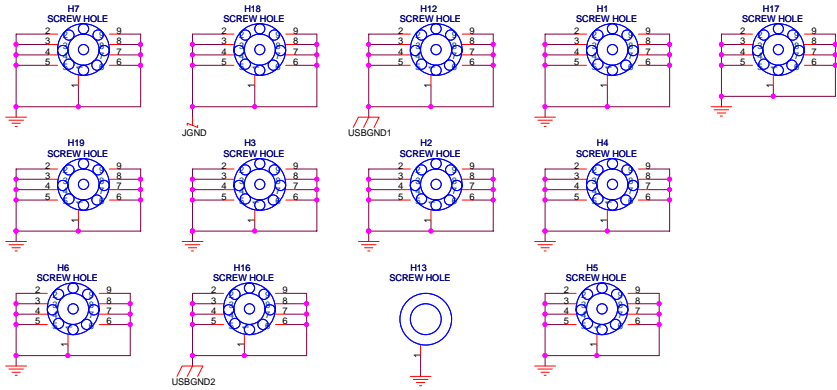
FS_A	FS_B	FS_C	CPU MHz	FSB
BSEL0	BSEL1	BSEL2		
1	0	1	100.00	400.00
1	0	0	133.33	533.00
1	1	1	200.00	
1	1	0	166.66	667.00
0	0	1	333.33	
0	0	0	266.66	
0	1	1	400.00	
0	1	0	200.00	

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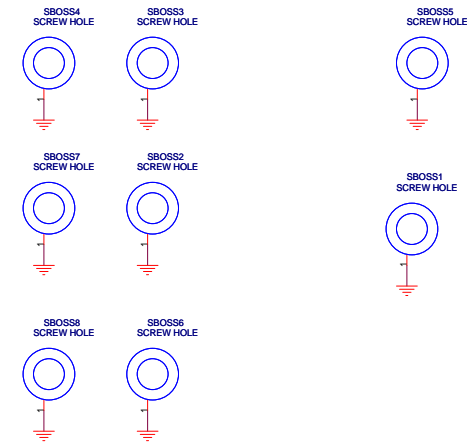
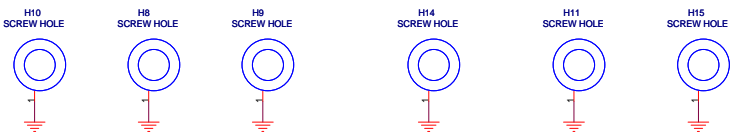
Title: **G420 CLOCK GENERATOR**

Size: Document Number
Date: 420-1-4-01
Thursday, August 03, 2006

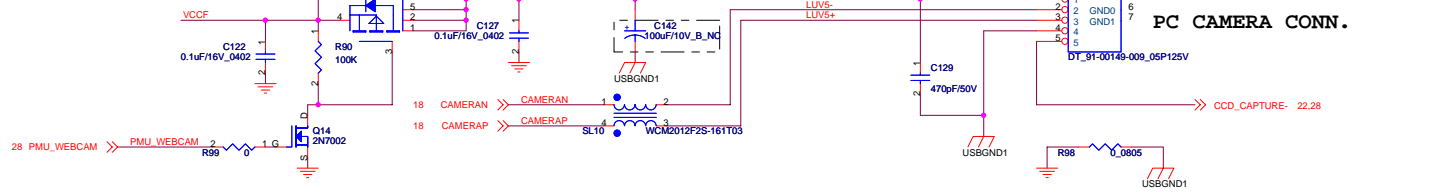
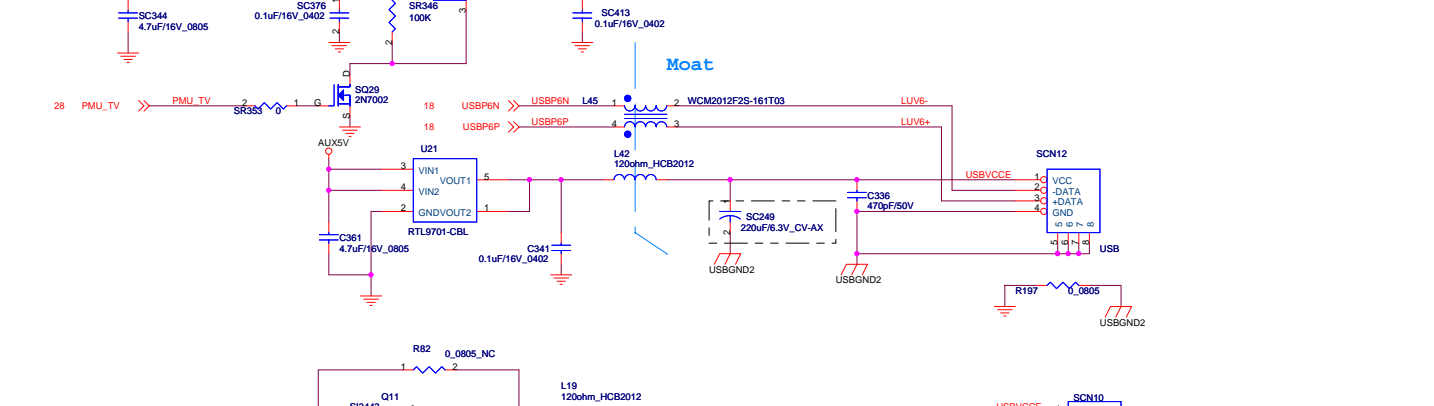
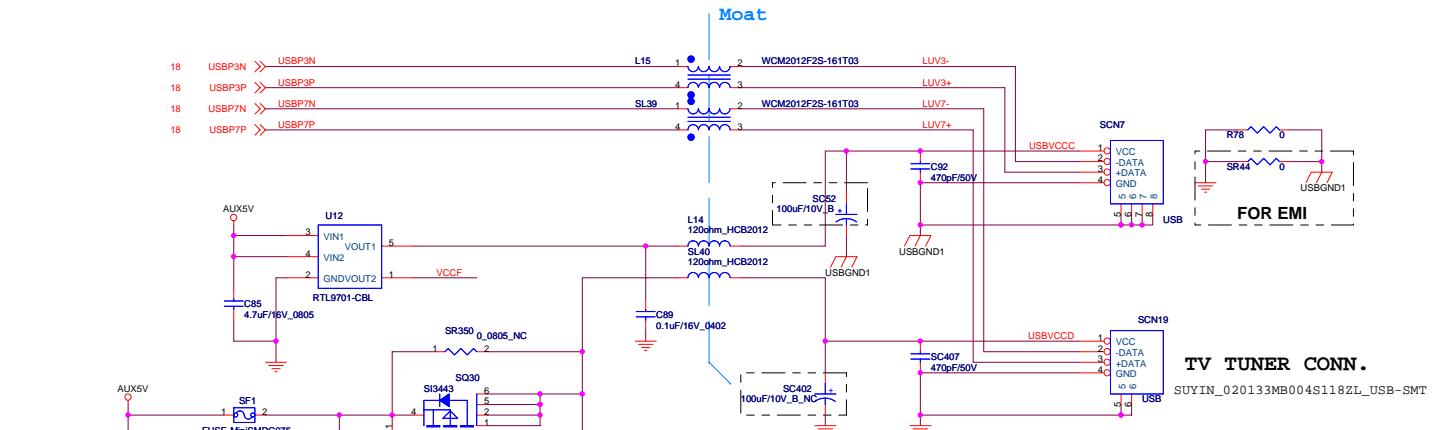
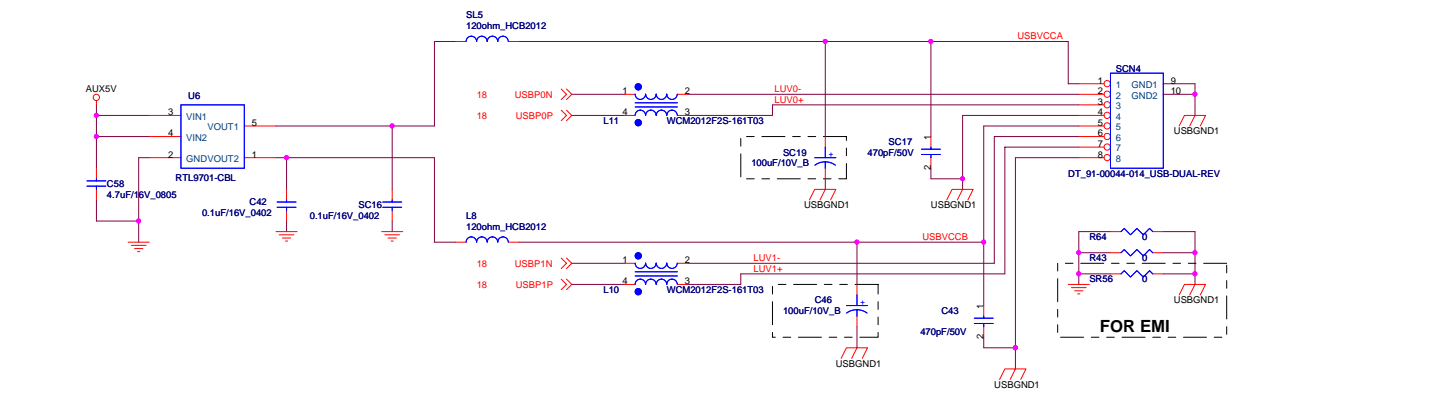
Rev: 3.0
Sheet: 14 of 44

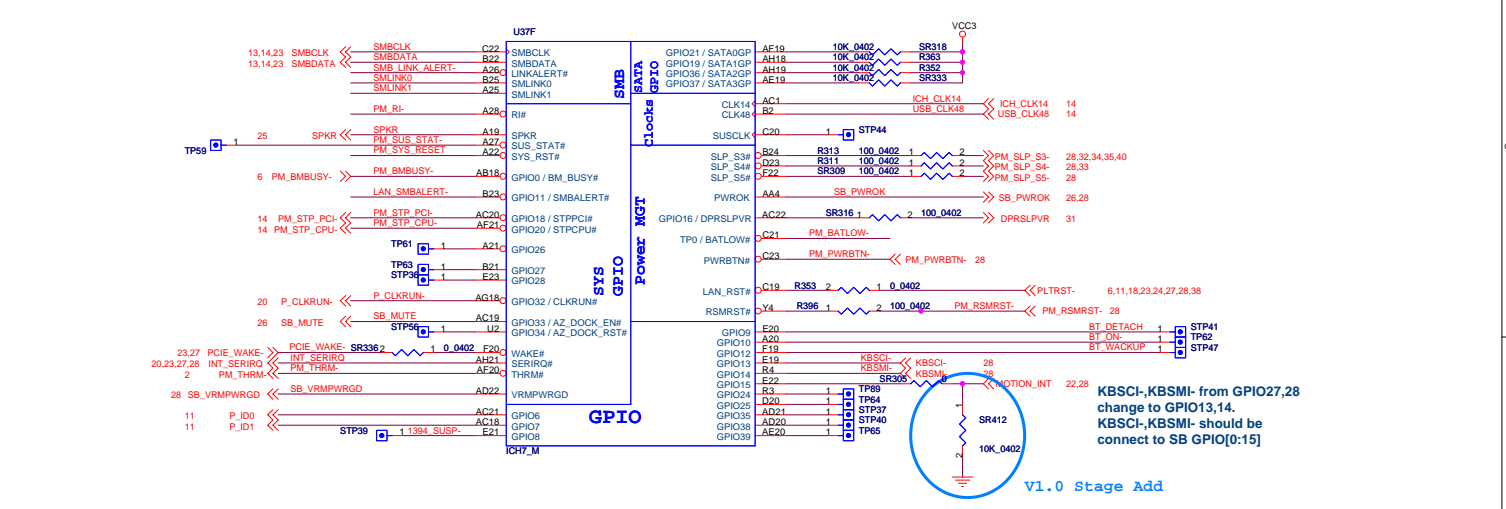
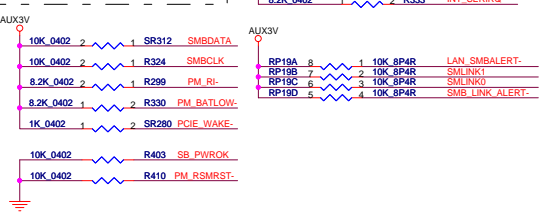
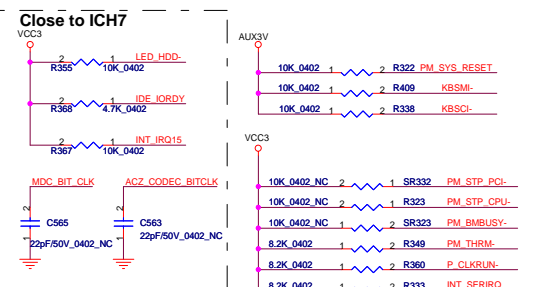
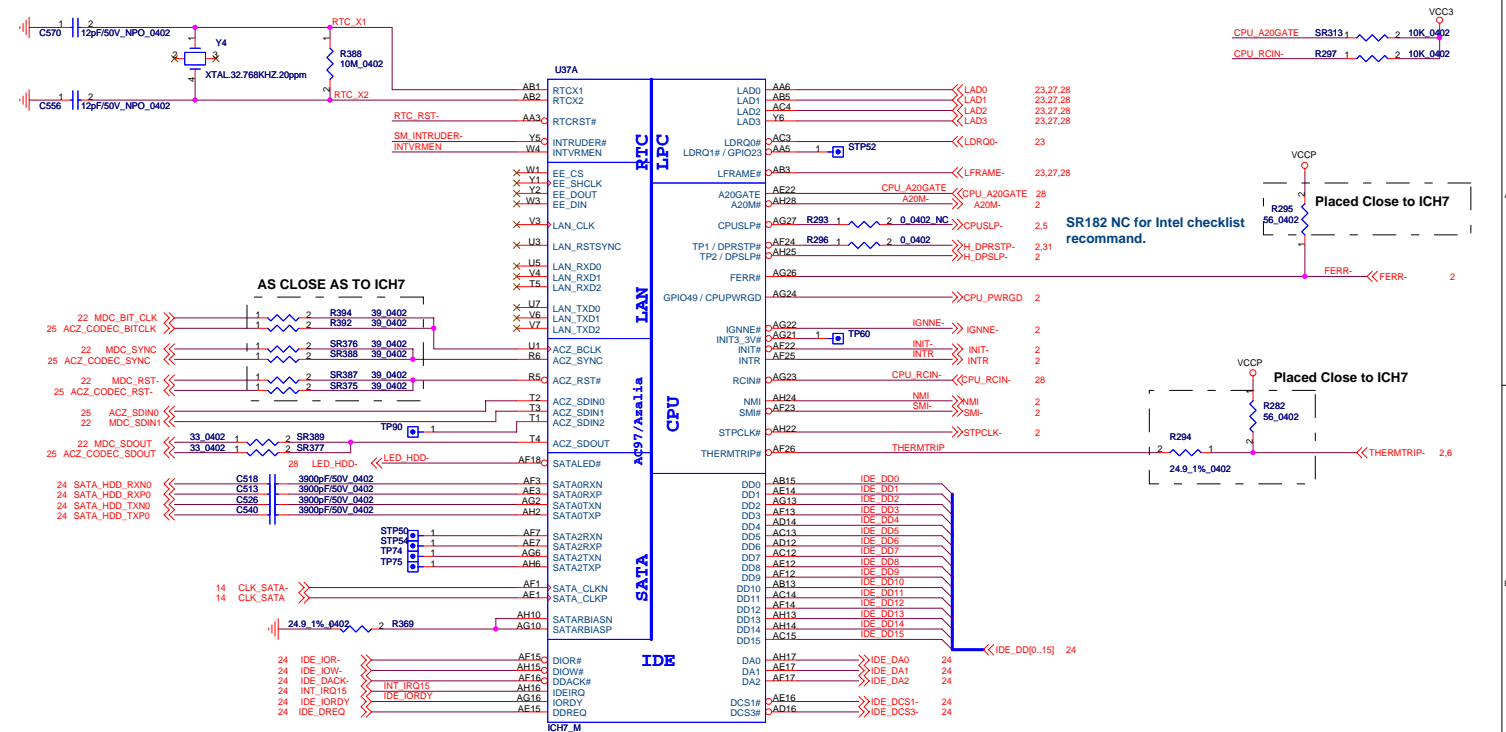
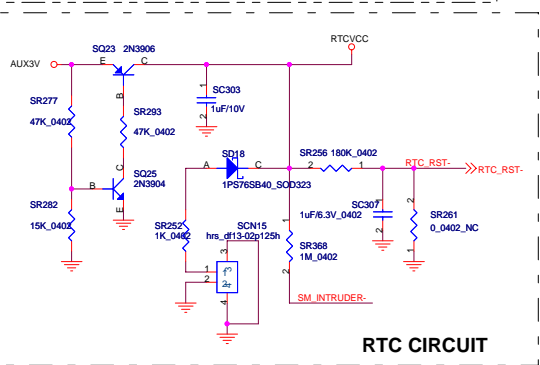
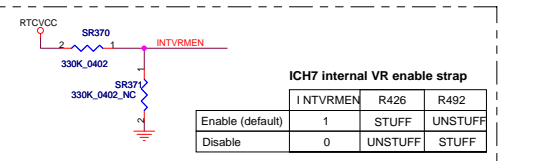


SYSTEM SCREW HOLE

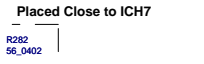
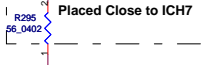


BOSS SCREW

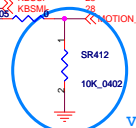




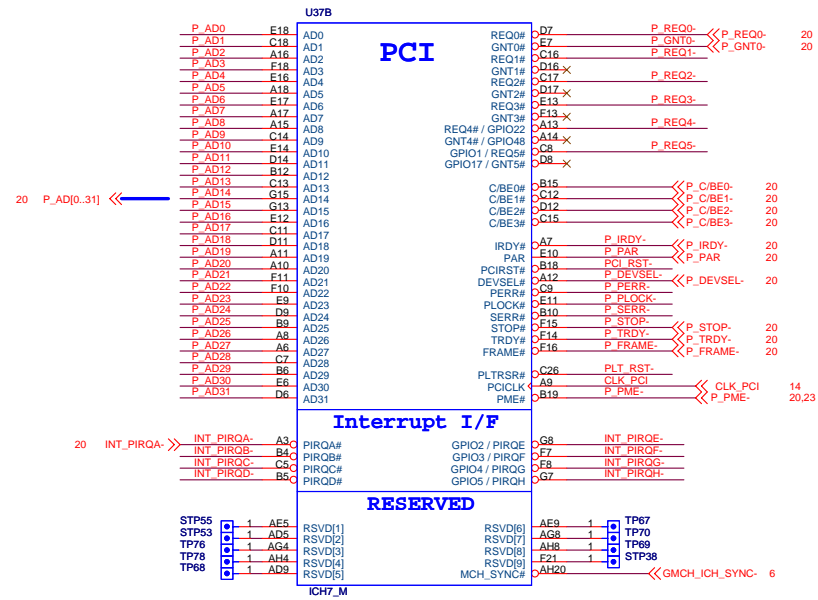
SR182 NC for Intel checklist recommend.



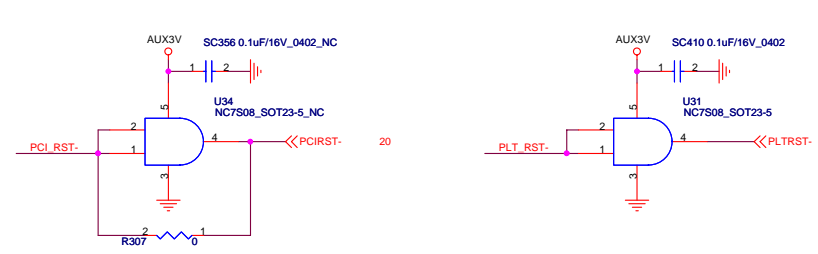
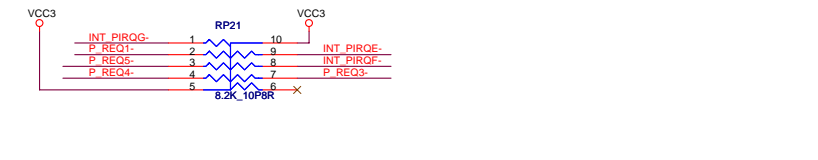
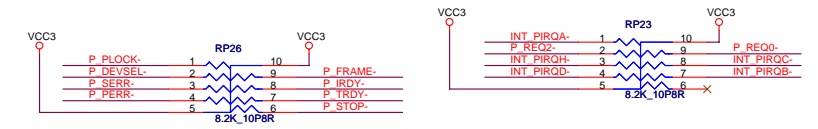
KBSCI-,KBSMI- from GPIO27,28 change to GPIO13,14. KBSCI-,KBSMI- should be connect to SB GPIO[0:15]



V1.0 Stage Add



USBP0N USBP0P USBP1N USBP1P	CN5 (DUAL CONNECT)	USB4N USB4P	NEW CARD
USB2N USB2P	Blue Tooth Wireless (Option)	USB5N USB5P	CAMERA
USB3N USB3P	CN6	USB6N USB6P	CN8
		USB7N USB7P	CN7



Layout note: C261 needs to be placed within 100mils of pin AD17 of ICH7 on the bottom side or 140 mils on the top

Layout note: C262 needs to be placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top

Layout note: Place above Caps within 100 mils of ICH on the bottom side or 140 mils on the top near D28, T28, AD28

Place within 100 mils of ICH on the bottom side or 140 mils on the top

Place within 100 mils of ICH on the bottom side or 140 mils on the top near pin AG5

Place within 100 mils of ICH on the bottom side or 140 mils on the top

Place within 100 mils of ICH on the bottom side or 140 mils on the top

Place within 100 mils of ICH on the bottom side or 140 mils on the top near AG9

Layout Note: Place at MCH edge

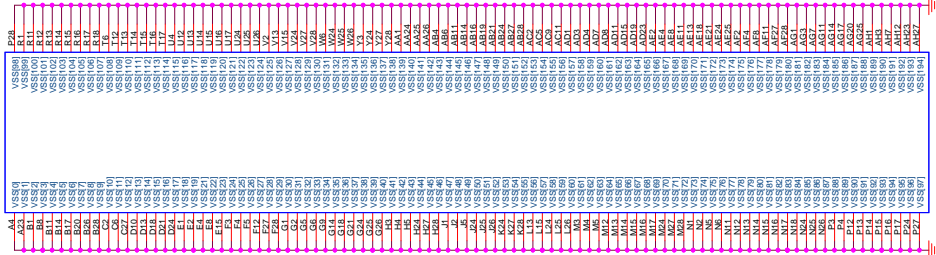
Layout Note: Place on secondary side under MCH

Place within 100 mils of ICH on the bottom side or 140 mils on the top near pin

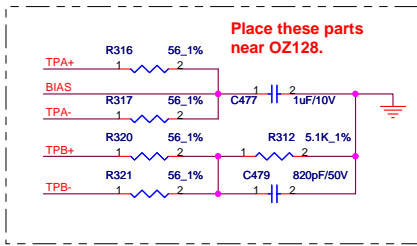
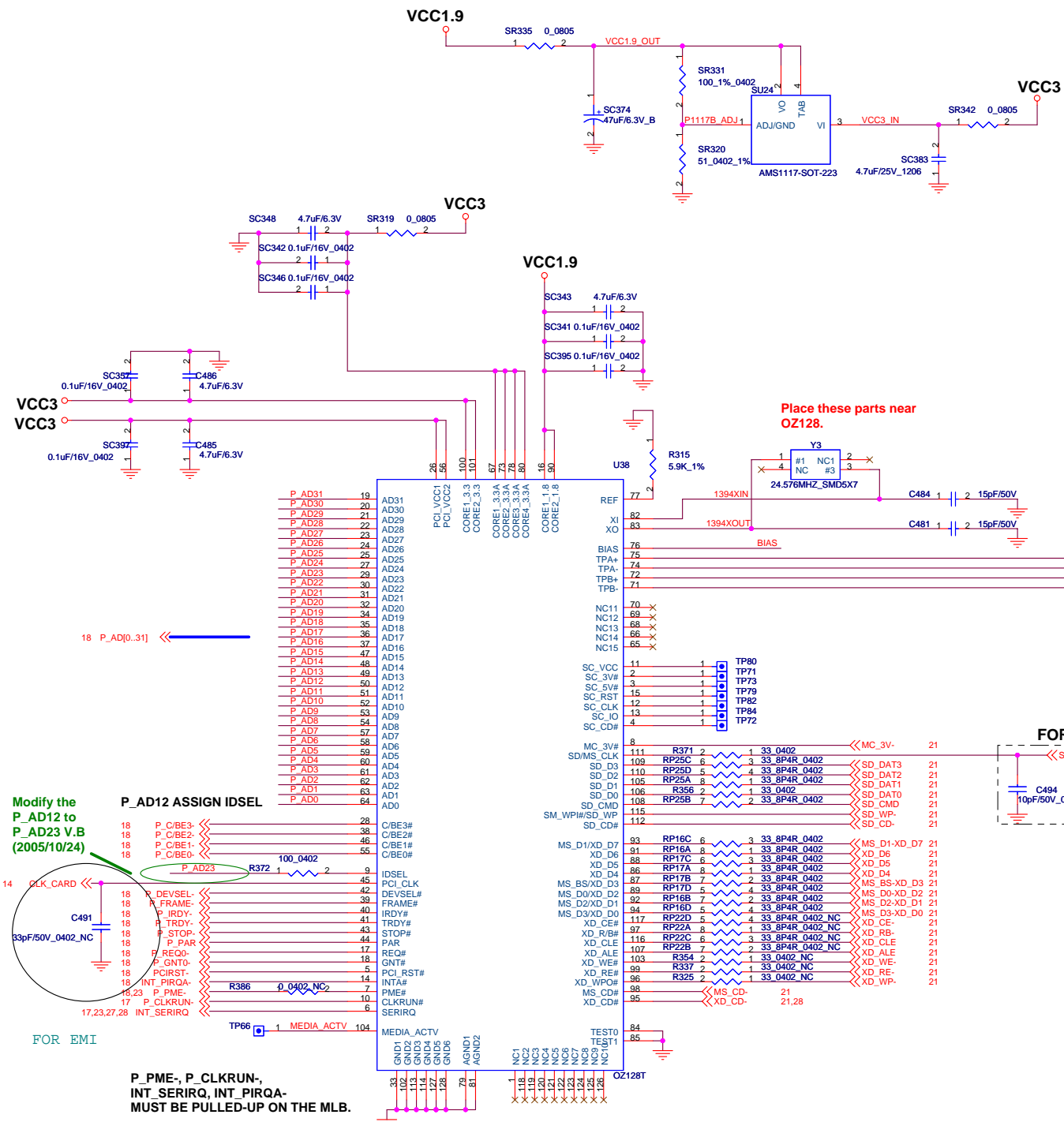
Place within 100 mils of ICH7 on the bottom side or 140 mils on the top near pin

Layout Note: Distribute in PCI section

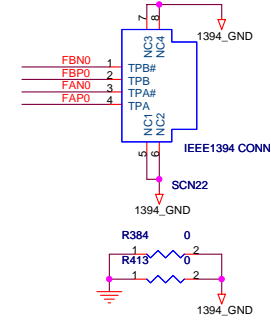
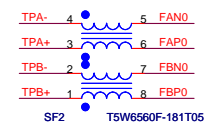
Place within 100 mils of ICH on the bottom side or 140 mils on the top

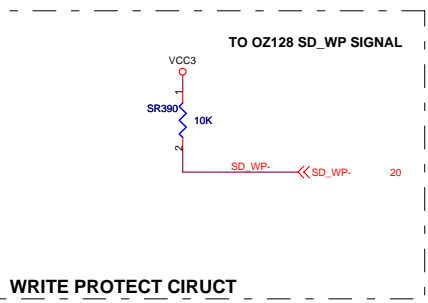
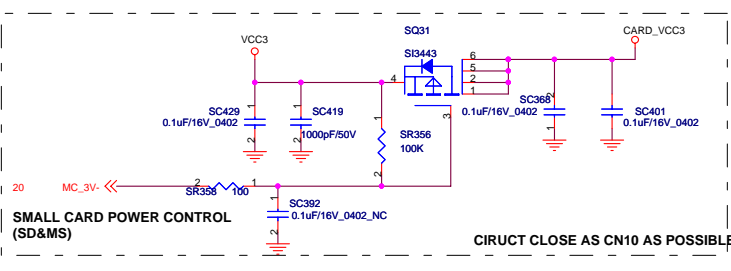
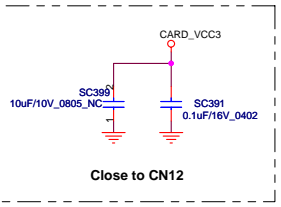
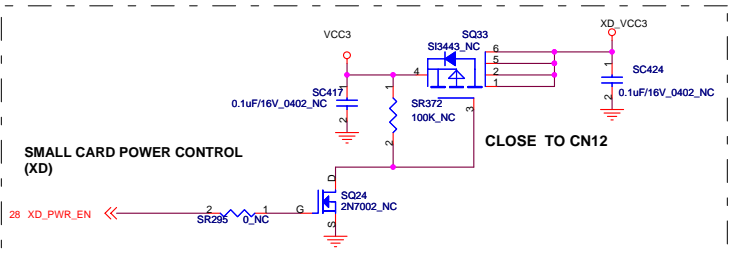
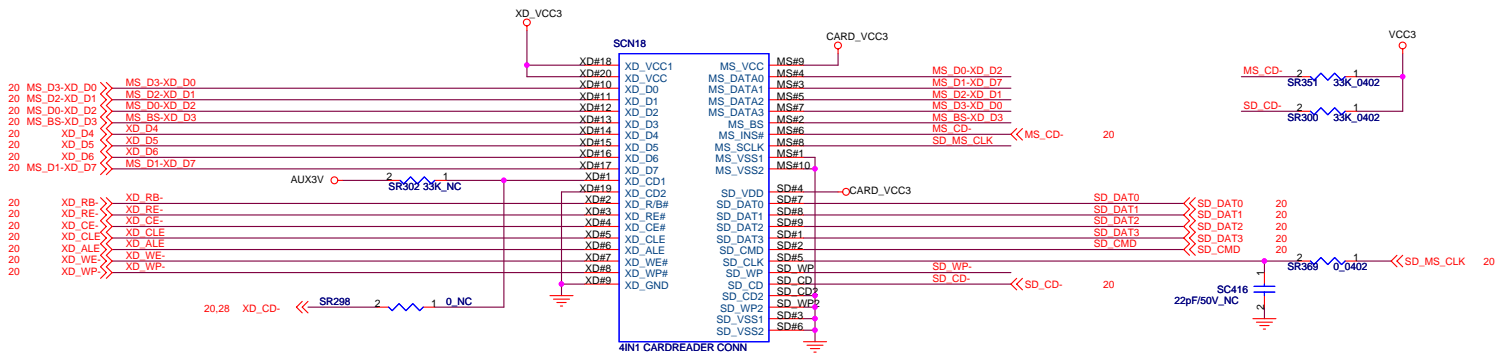


Elitegroup Computer Systems logo and title block containing document information: Title: G420 ICH7-M(POWER & GND), Size: Custom, Document Number: 420-1-4-01, Rev: 3.0, Date: Thursday, August 03, 2006, Sheet: 19 of 44.



NOTE 2: These 1394 signals are high speed differential pairs and must be kept equal length with a differential impedance (Z_0) of 110ohms.





CARD READER EC FUNCTION TABLE

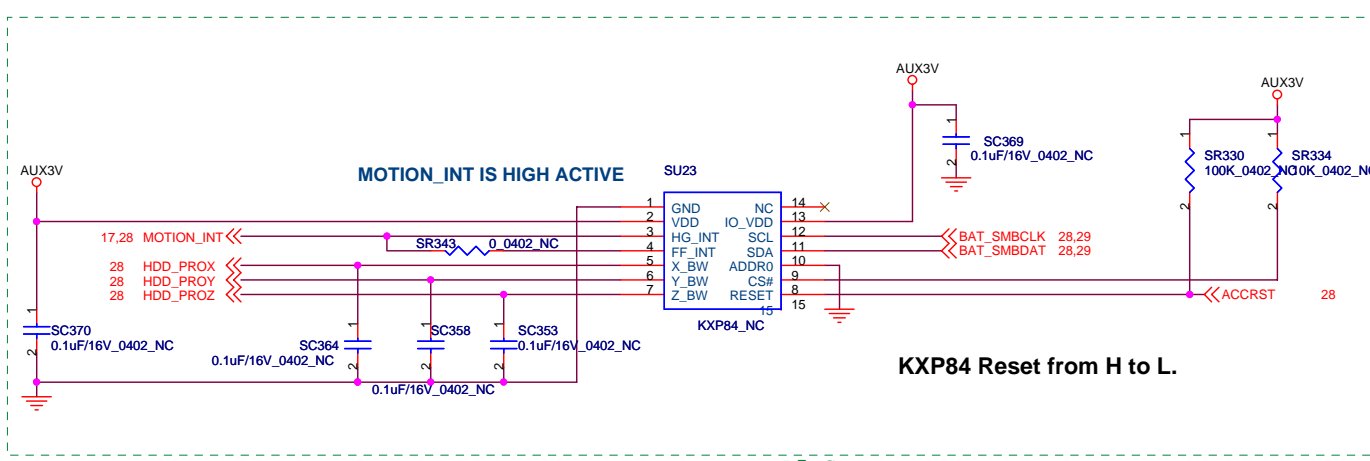
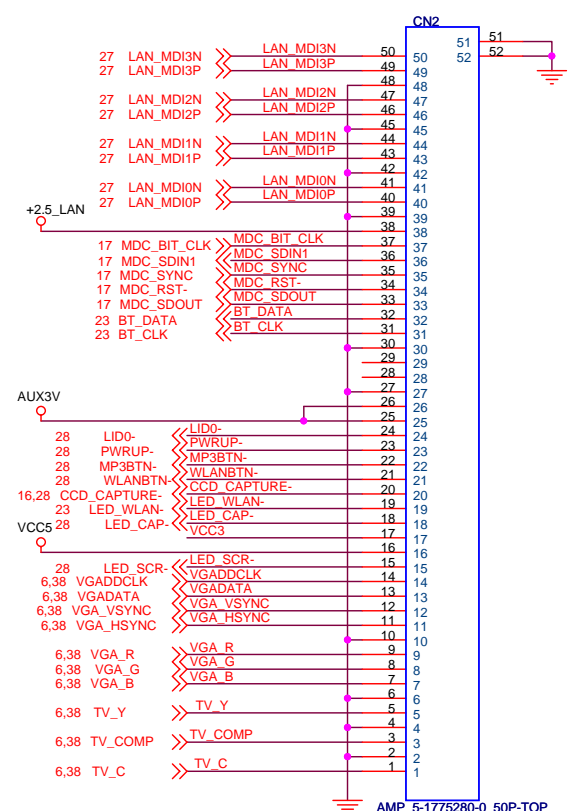
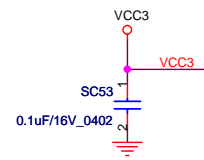
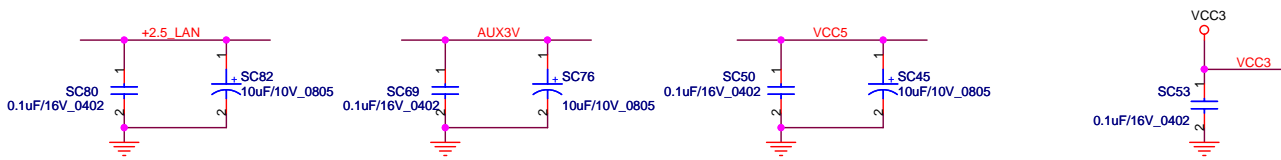
	SD	SD LOCK	SD UNLOCK
XD_CD-	L	H	H
XD_PWR_EN (OUT)	H	L	L
SD_WP- (OUT)	H	H	H to L

Elitegroup Computer Systems

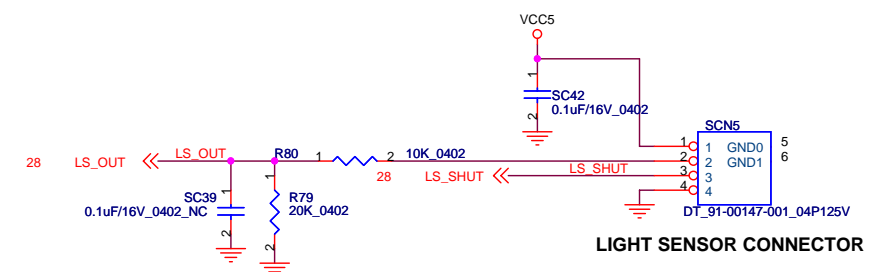
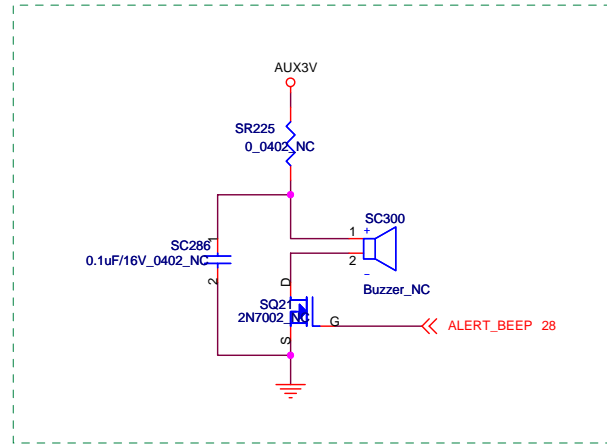
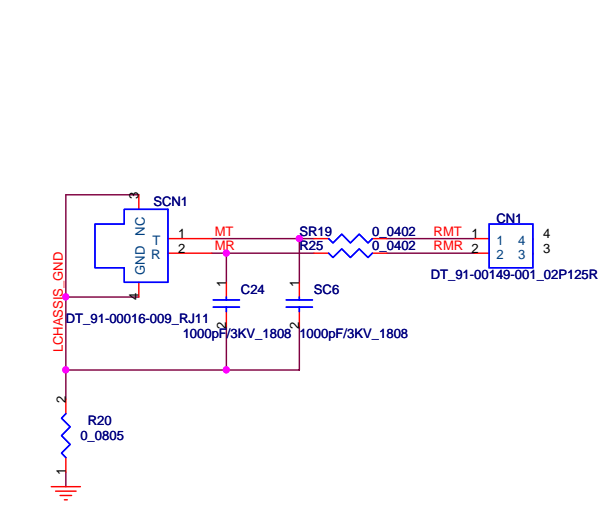
Title: **G420 CARDREADER CONNECT**

Size: Custom | Document Number: 420 -1-4-01 | Rev: 3.0

Date: Thursday, August 03, 2006 | Sheet: 21 of 44



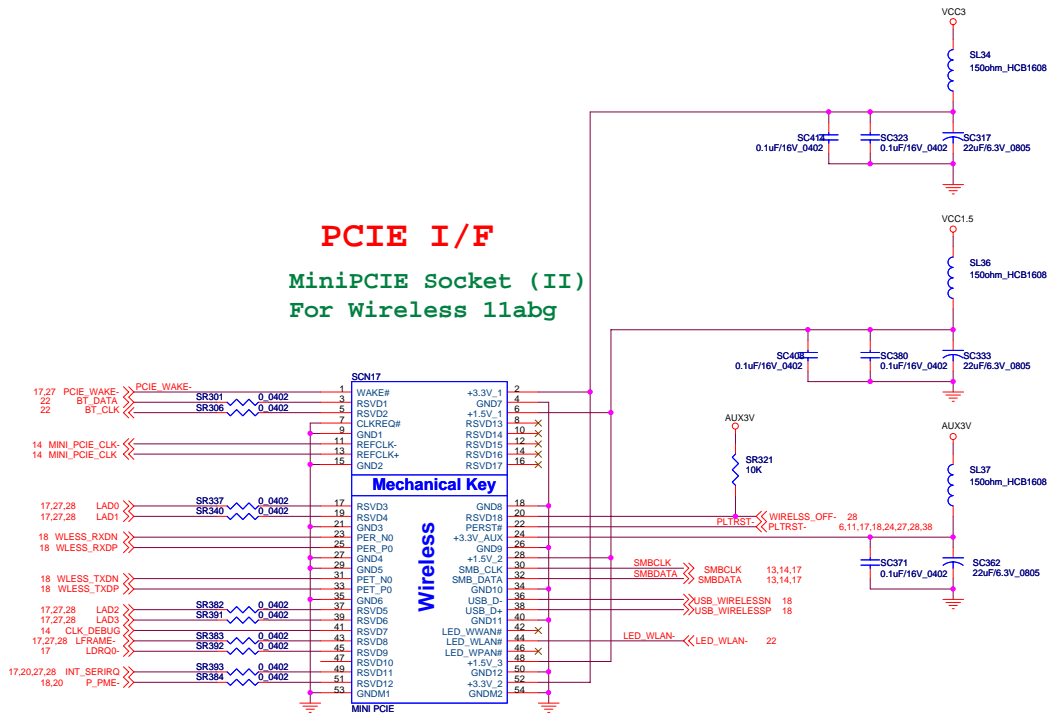
A5 Stage remove
HDD protection and alert function



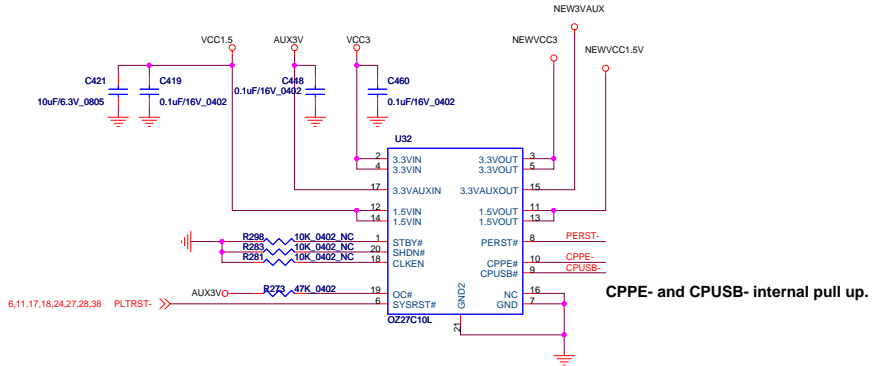
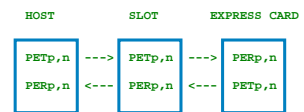
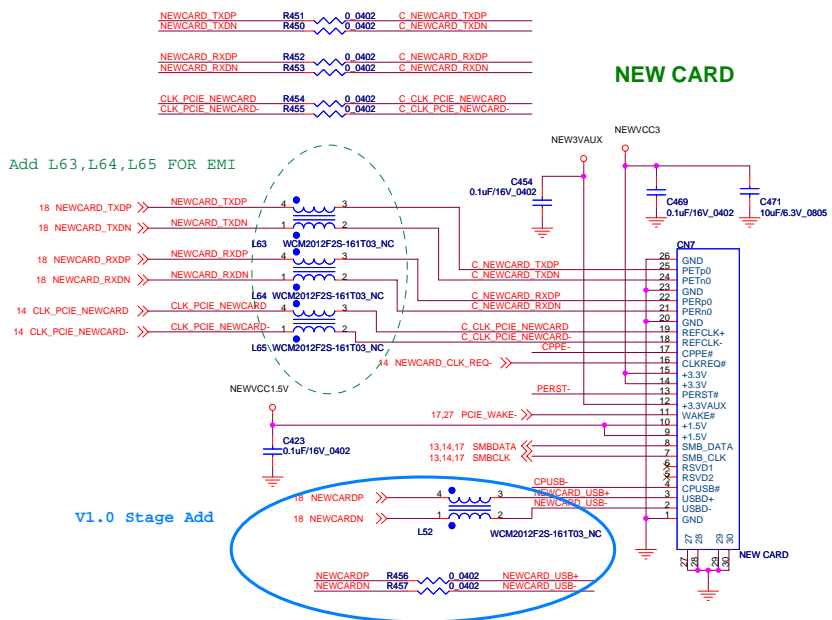
Elitegroup Computer Systems		
G420 RJ11/IO/LIGHT SENSOR CONNECT		
Title		
Size B	Document Number	Rev
	420 -1-4-01	3.0
Date:	Thursday, August 03, 2006	Sheet 22 of 44

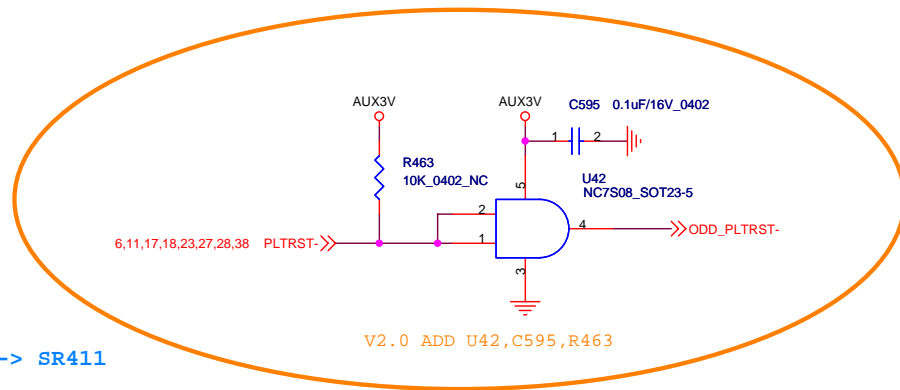
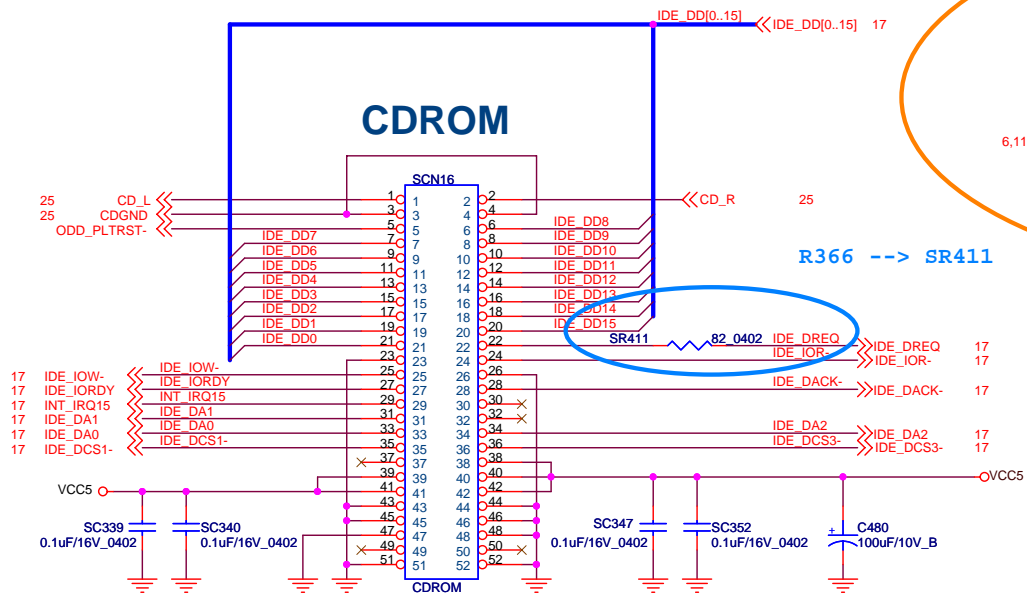
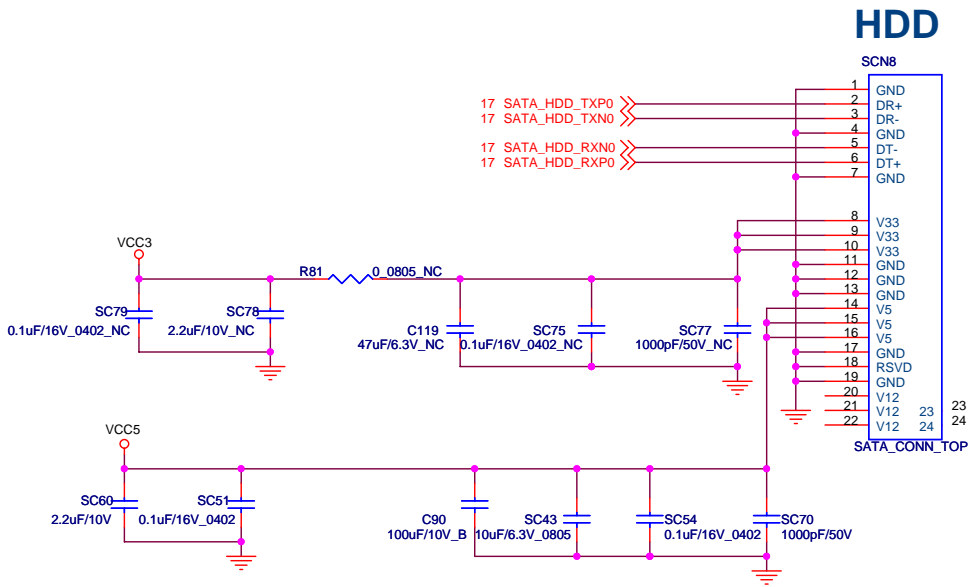
PCIE I/F

MiniPCIE Socket (II) For Wireless 11abg

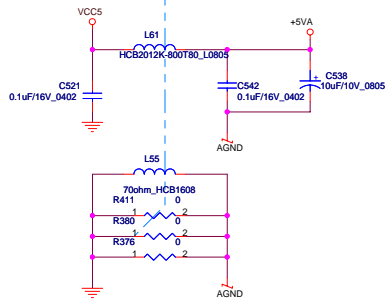


A5 Stage Add L63,L64,L65 FOR EMI



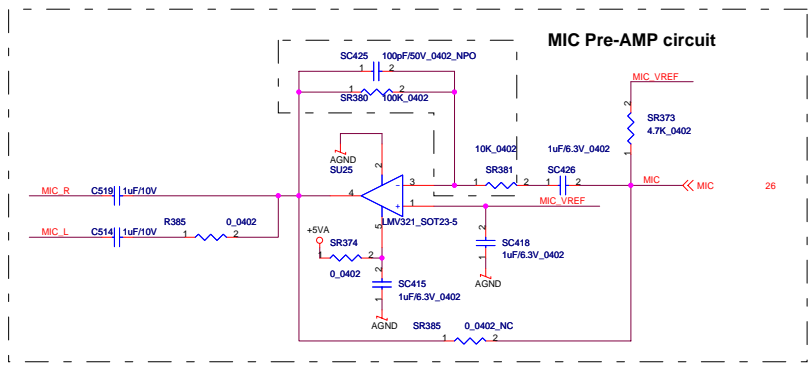


ECS Elitegroup Computer Systems		
Title G420 HDD & CDROM CONN		
Size B	Document Number 420 -1-4-01	Rev 3.0
Date: Thursday, August 03, 2006	Sheet 24	of 44

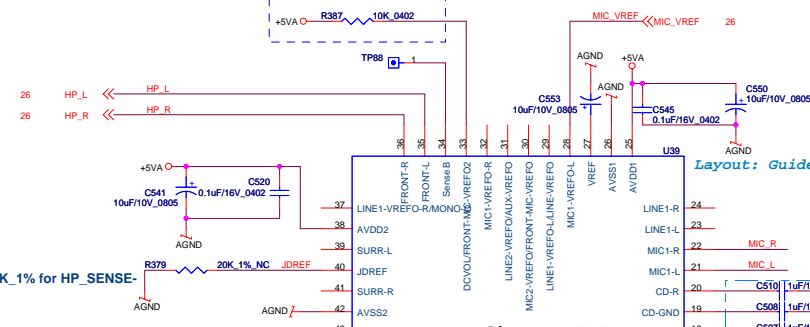


Layout: Moat 50mils

10K ohm for improving power ON pop noise.



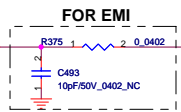
MIC Pre-AMP circuit



Add SR49 20K_1% for HP_SENSE.

HD Audio: ALC880H

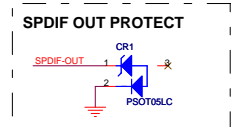
Layout: Guide with GND in Digital Zone



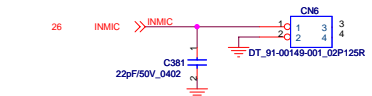
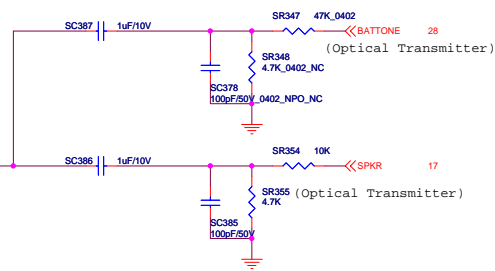
Pin 47 & Pin 48 are Digital separate into digital area.

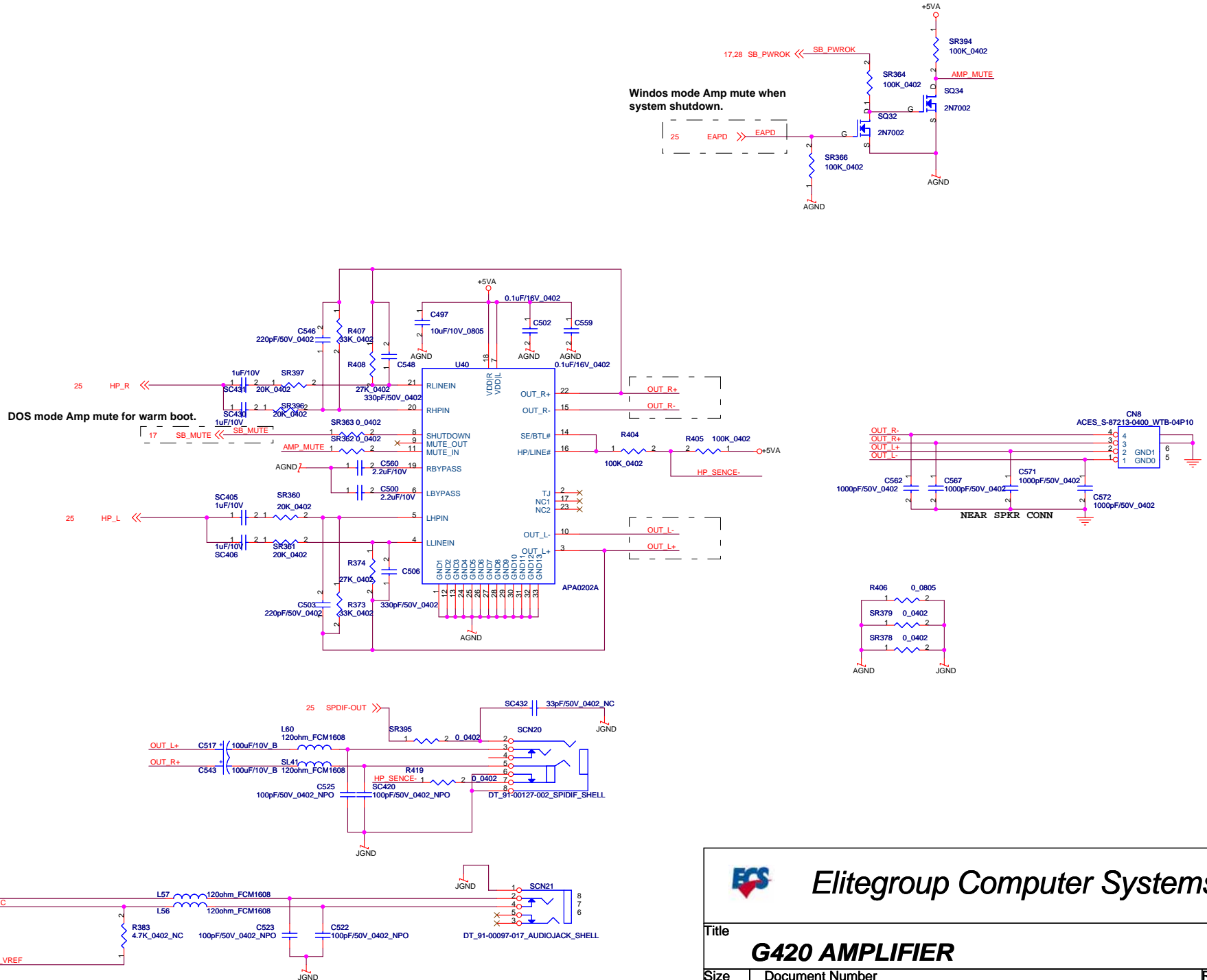
Spilt by DGND

Layout: Moat 50mils



SPDIF OUT PROTECT



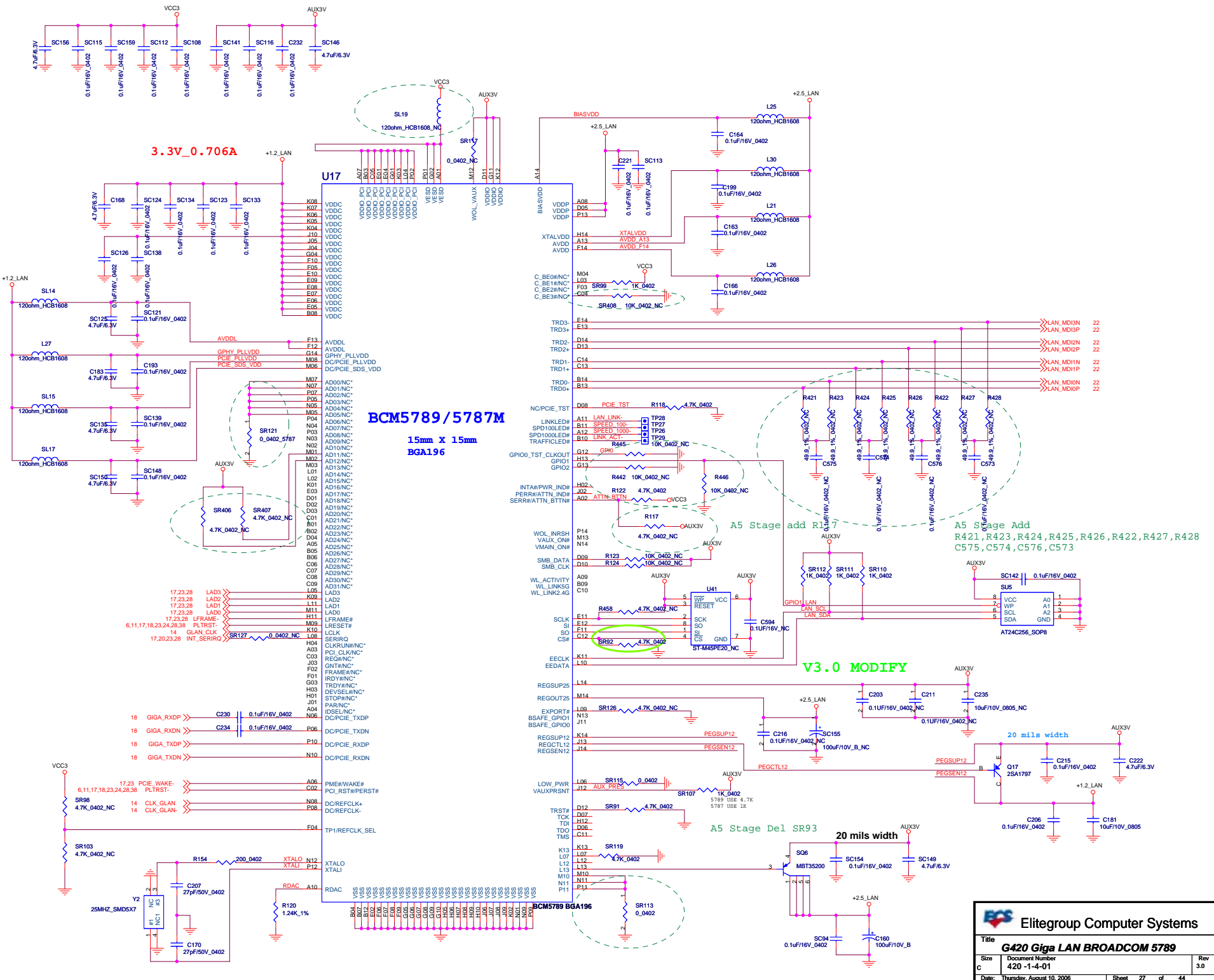


Windows mode Amp mute when system shutdown.

DOS mode Amp mute for warm boot.



Title		
G420 AMPLIFIER		
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BCM5789/5787M
 15mm X 15mm
 BGA196

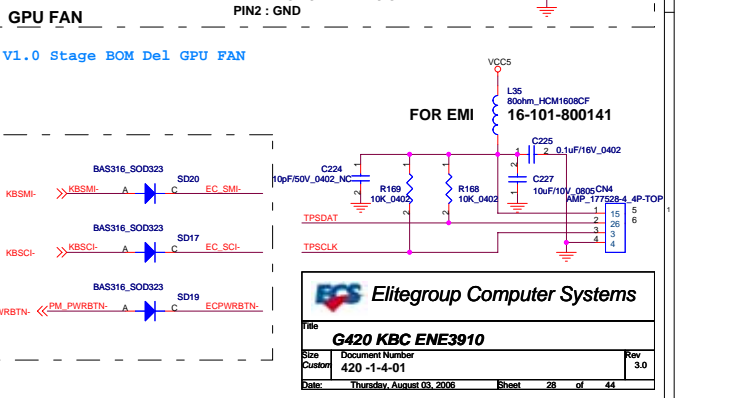
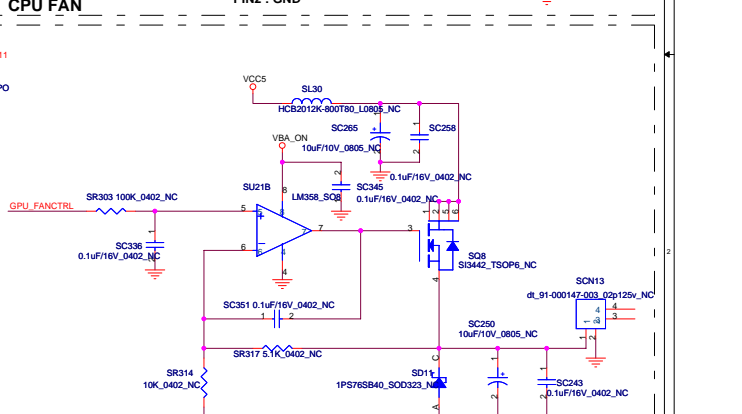
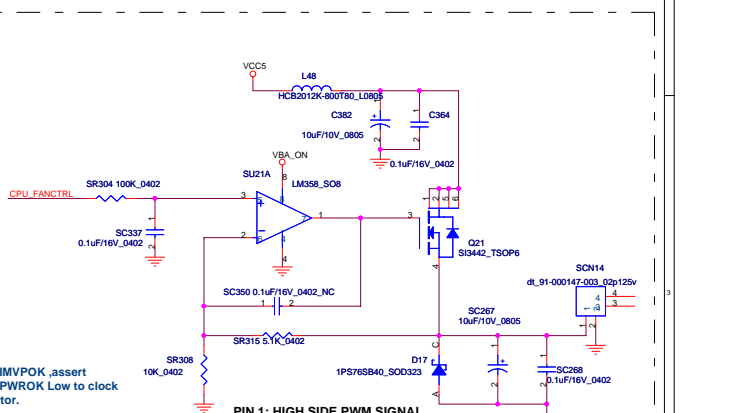
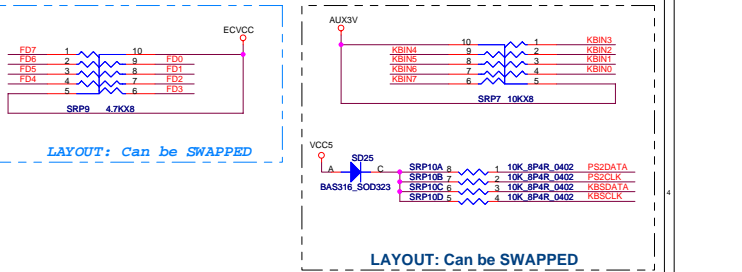
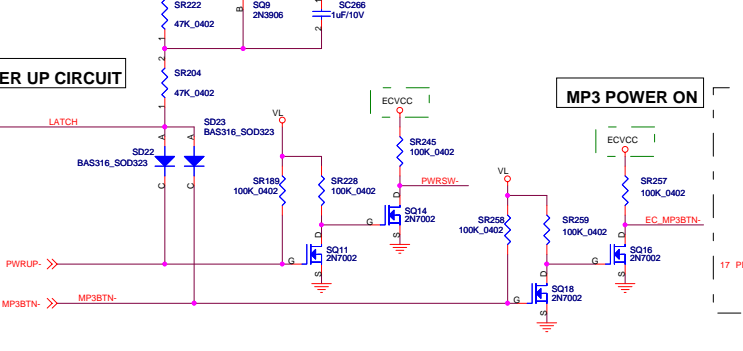
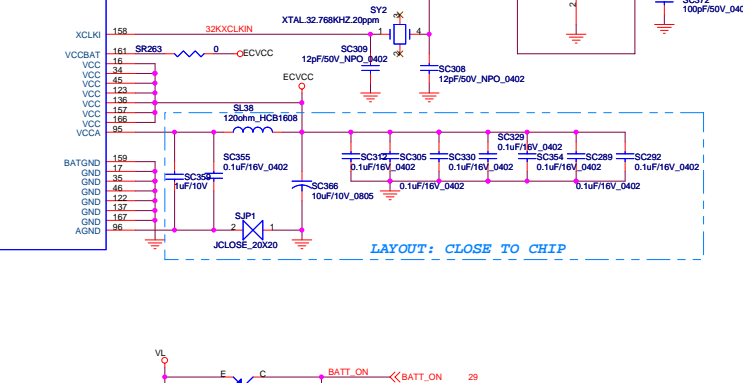
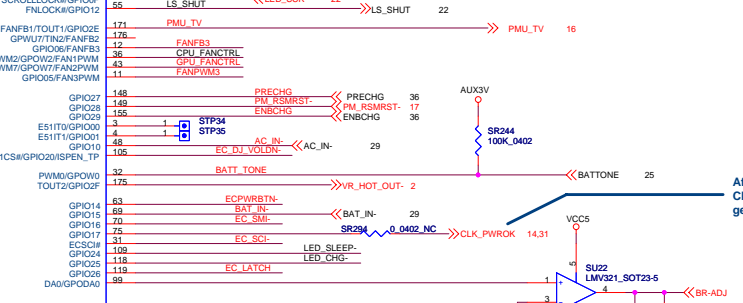
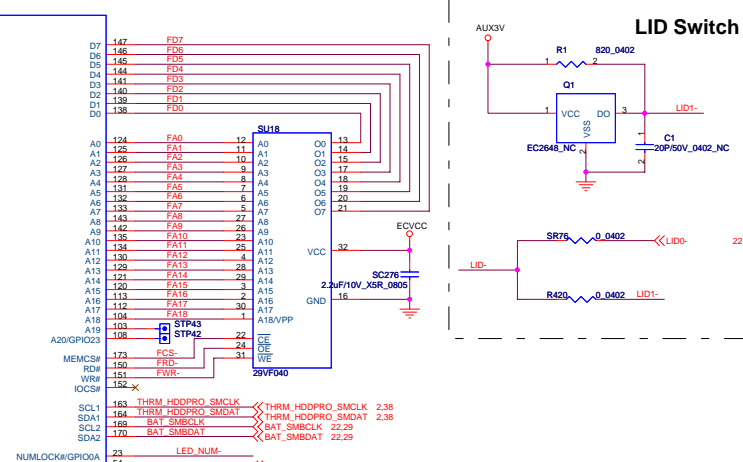
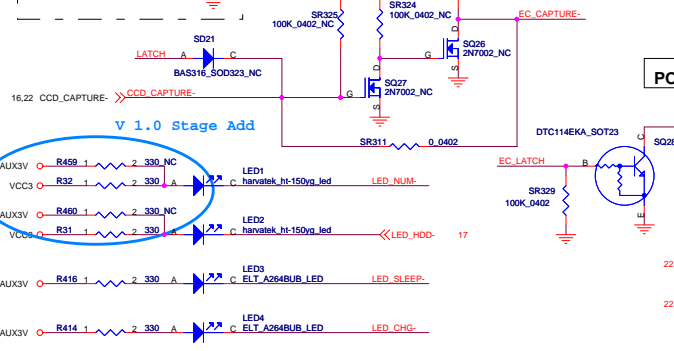
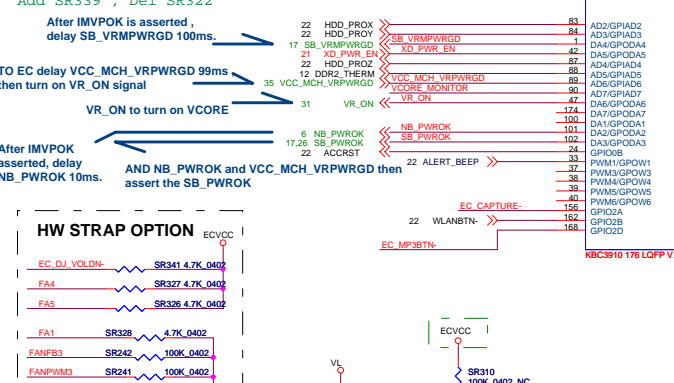
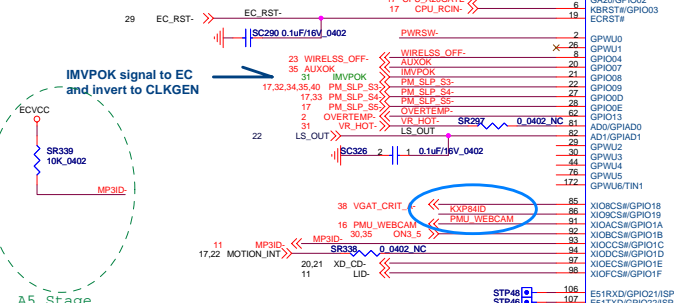
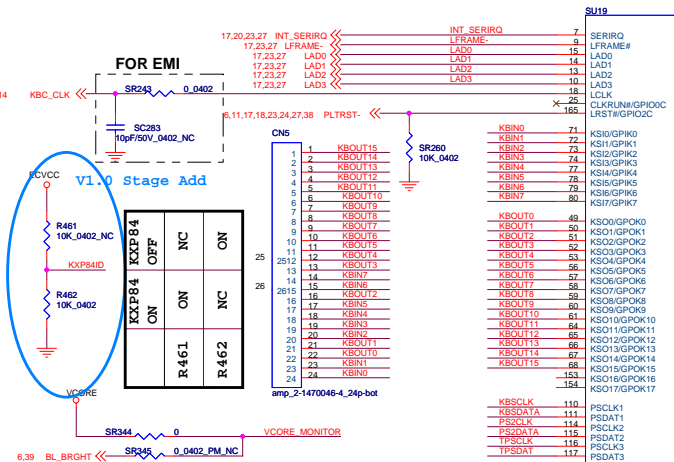
V3.0 MODIFY

A5 Stage Del SR93

A5 Stage add R17

A5 Stage Add R421, R423, R424, R425, R426, R422, R427, R428 C575, C574, C576, C573

Elitegroup Computer Systems		
Title		
G420 Giga LAN BROADCOM 5789		
Size	Document Number	Rev
c	420 -1-4-01	3.0
Date:	Thursday, August 10, 2006	Sheet 27 of 44

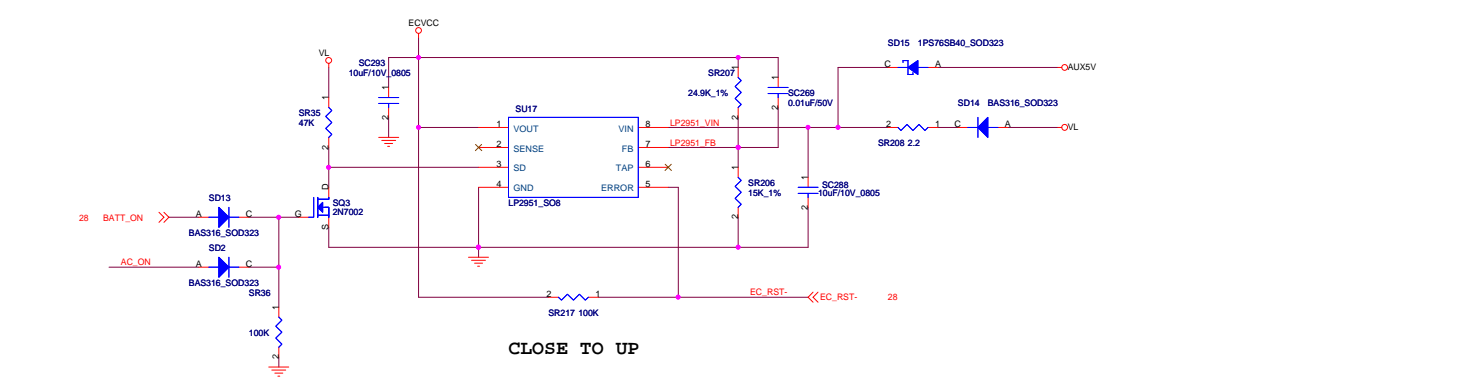
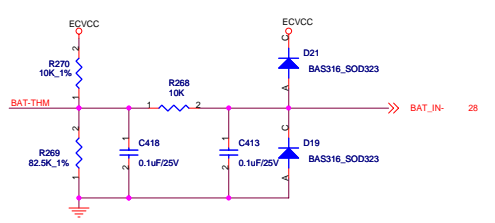
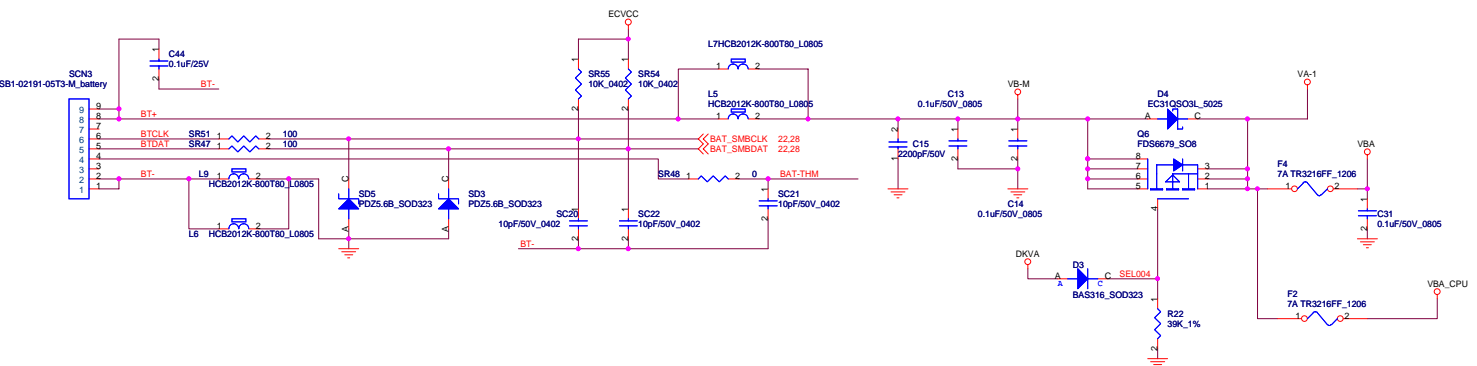
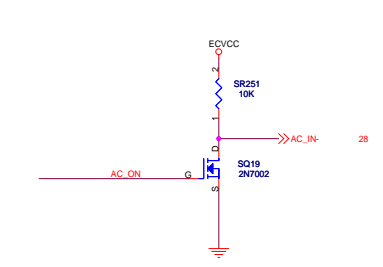
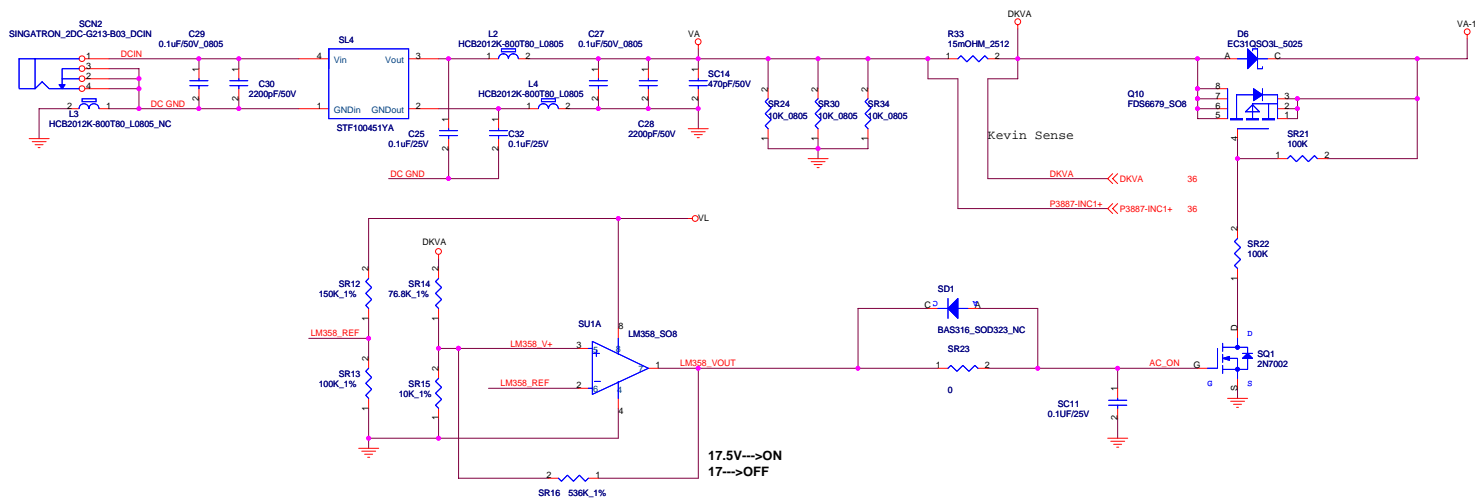


Elitegroup Computer Systems

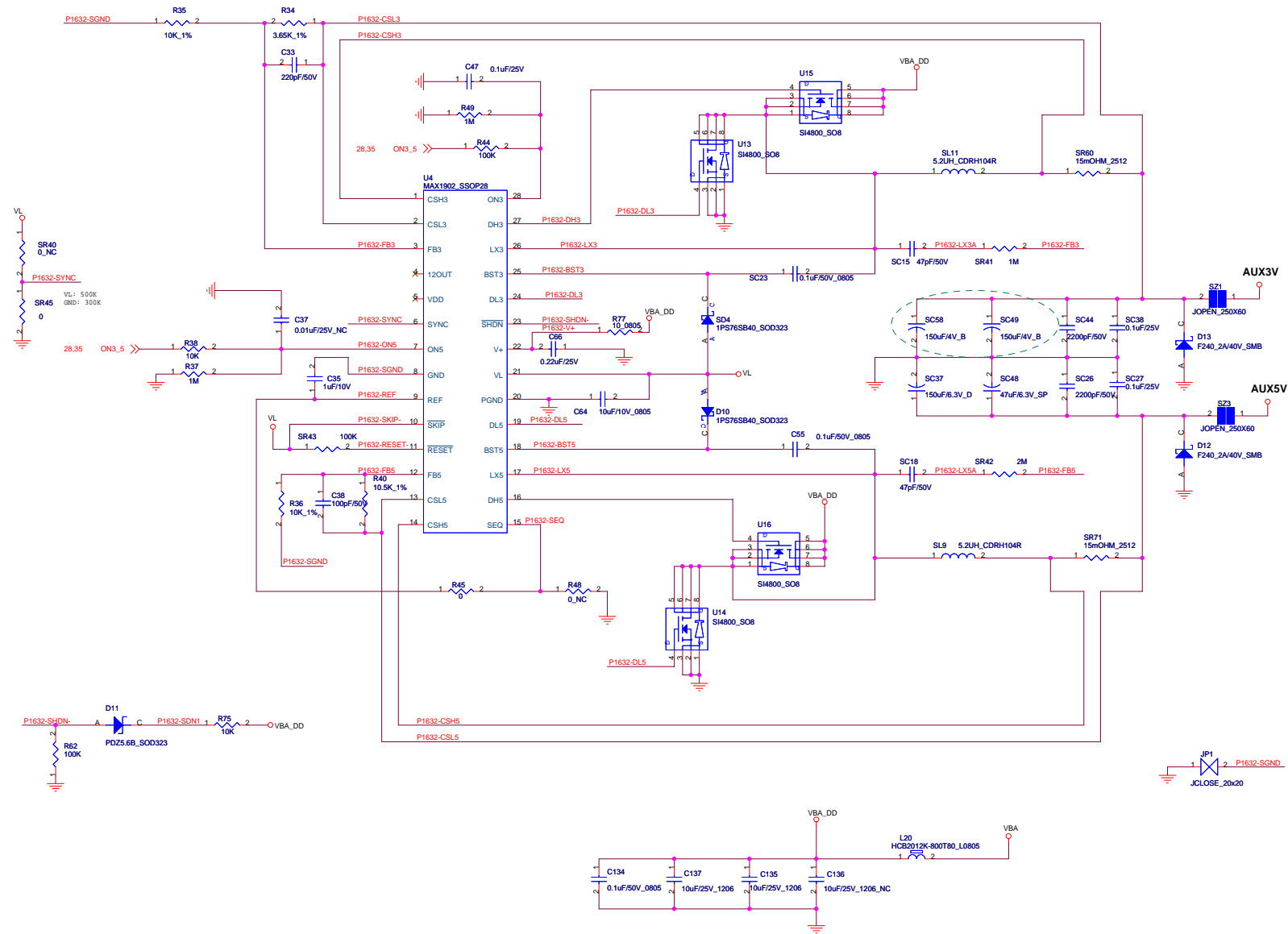
G420 KBC ENE3910

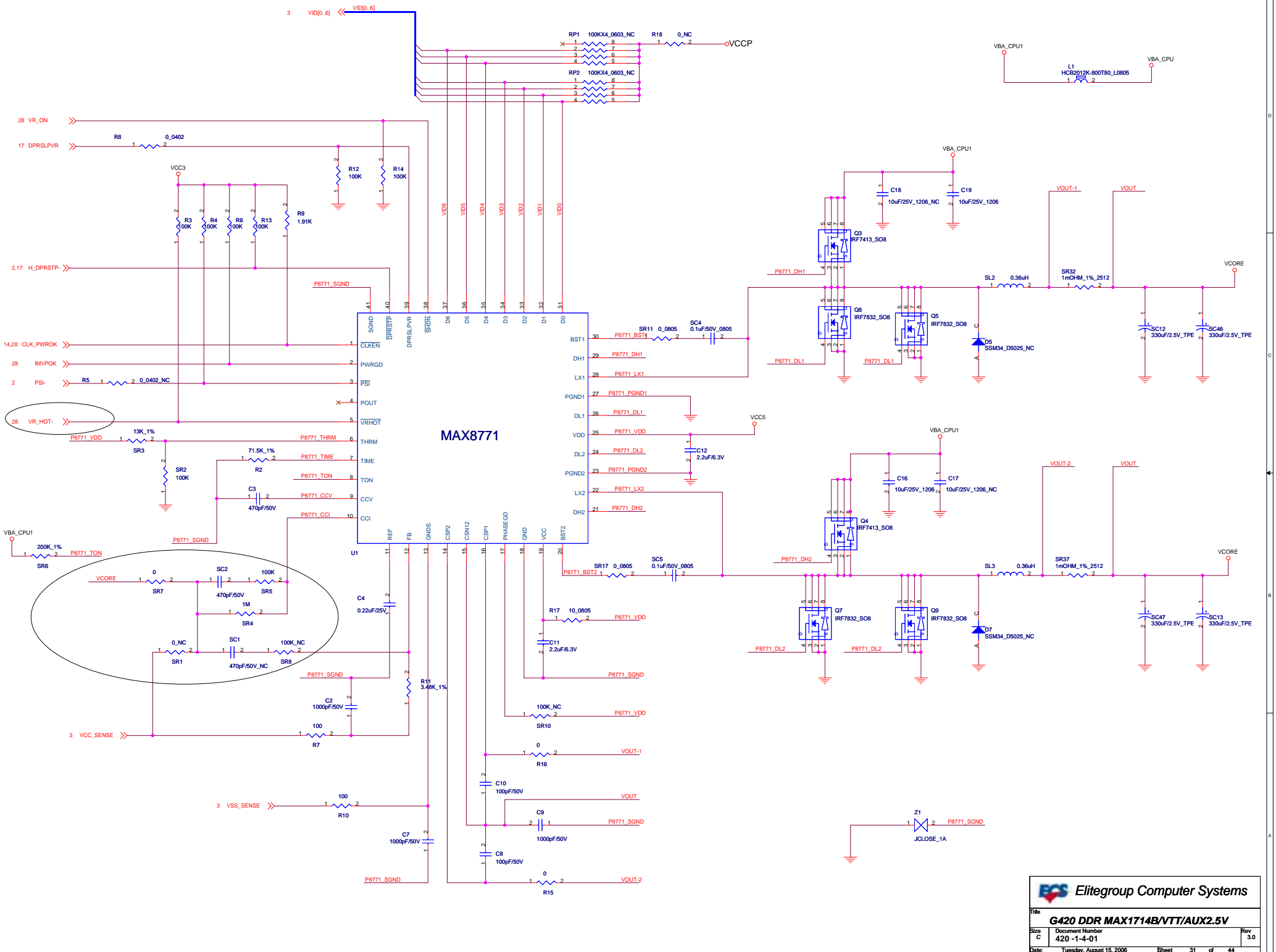
File: **G420 KBC ENE3910**
 Size: **420-1-4-01**
 Date: **Thursday, August 03, 2006**

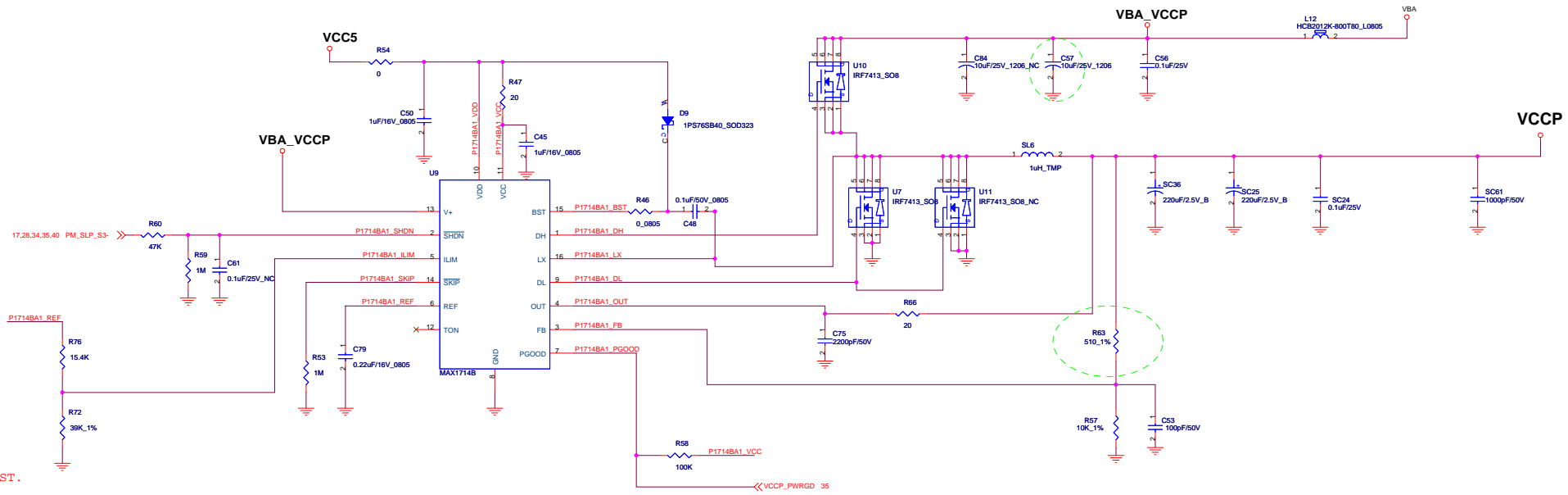
Document Number: **420-1-4-01**
 Sheet: **28** of **44**



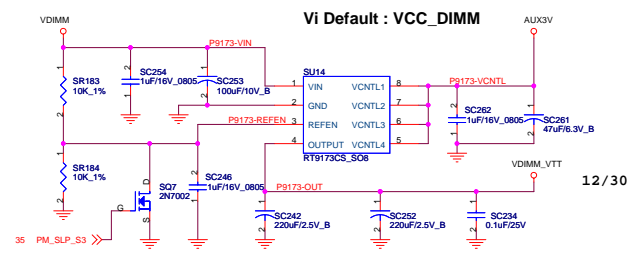
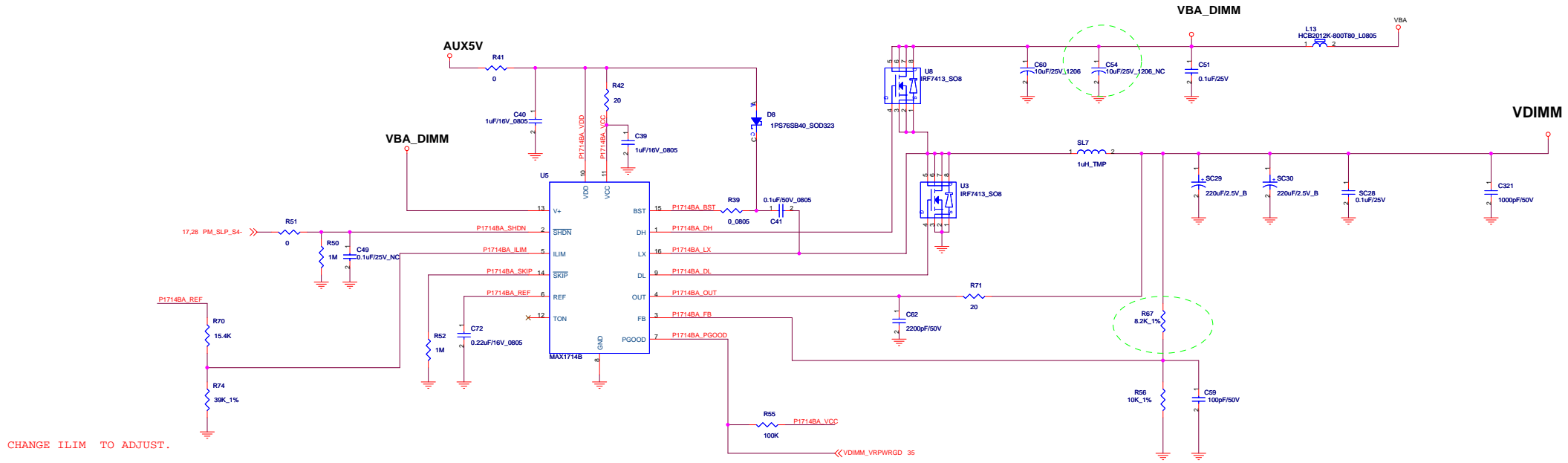
CLOSE TO UP





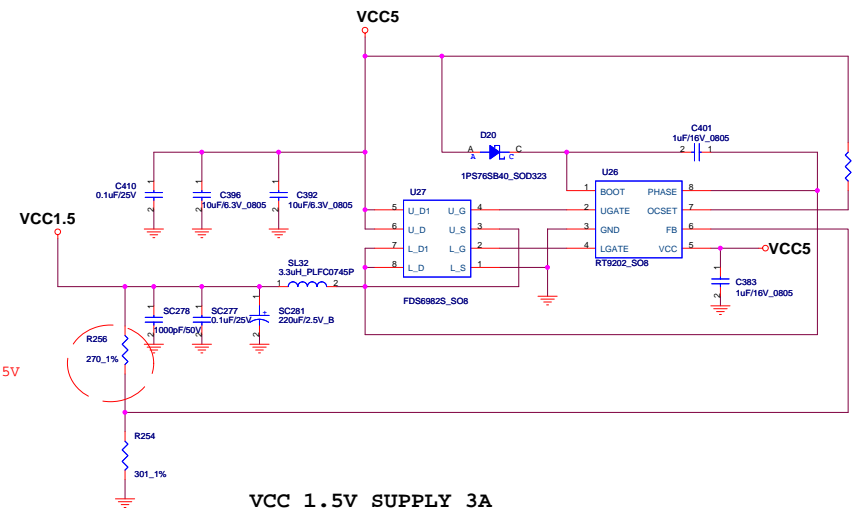


CHANGE ILIM TO ADJUST.

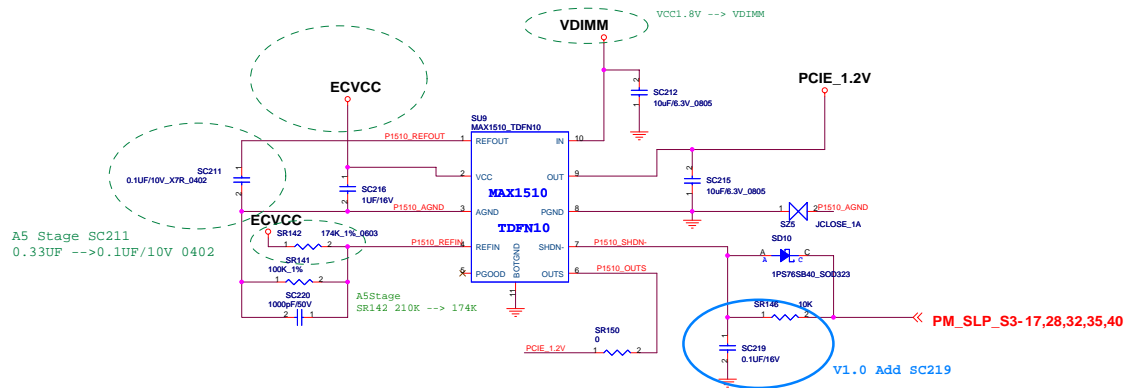
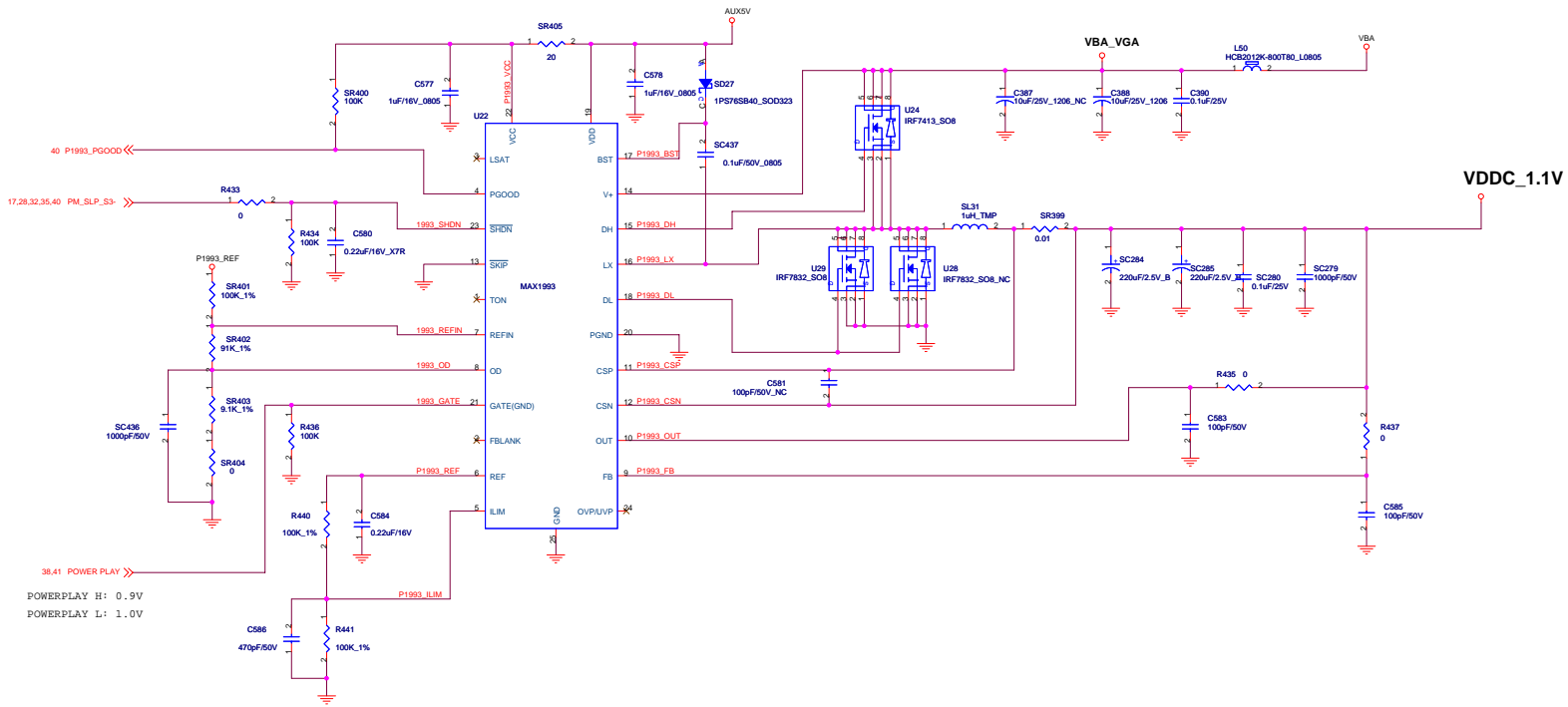


DIMM_1.8V SUPPLY 3.5A & VTT0.9V 1A FOR DDR

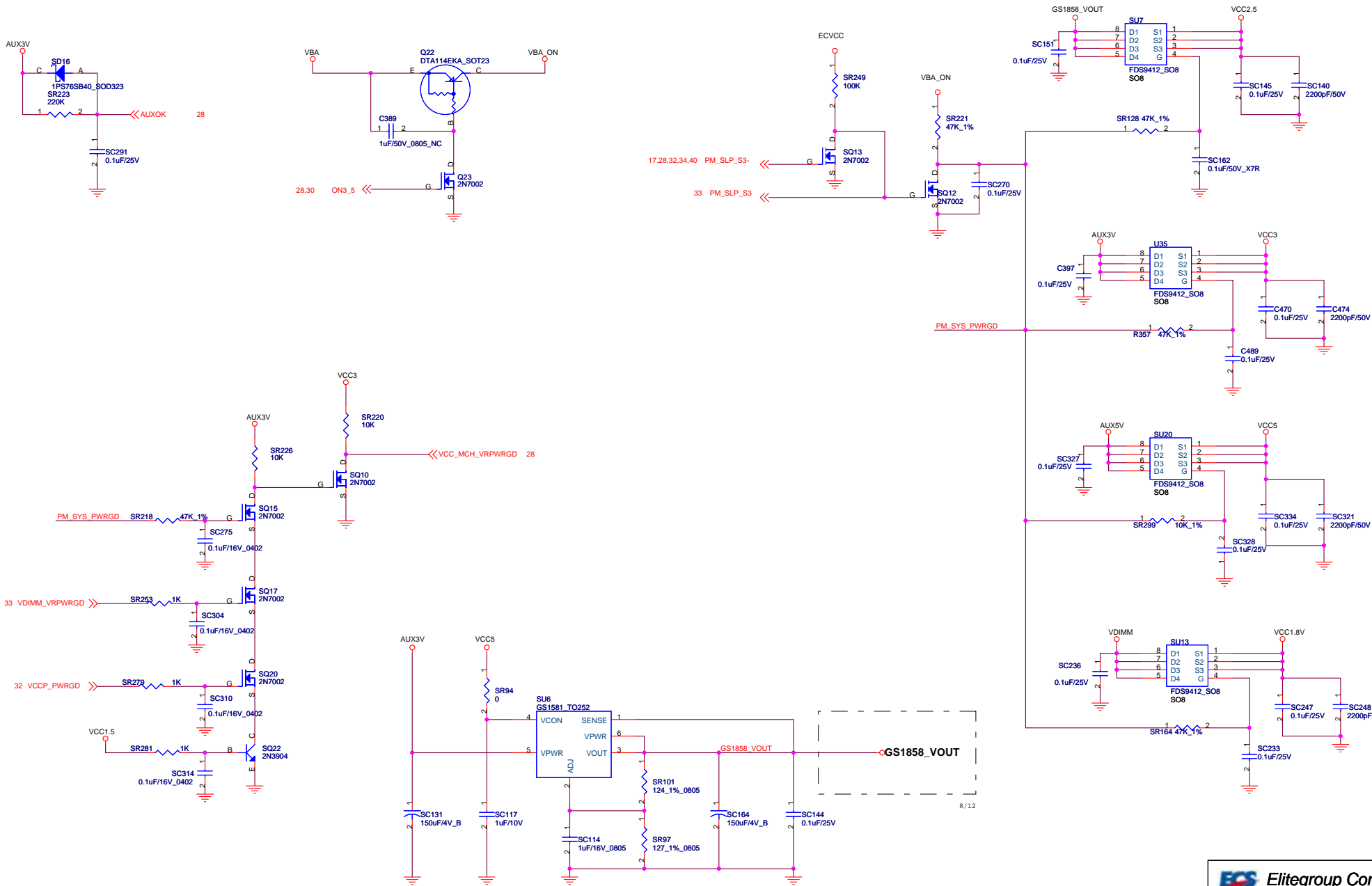
R256=270 OHM VOUT=1.5V



VCC 1.5V SUPPLY 3A



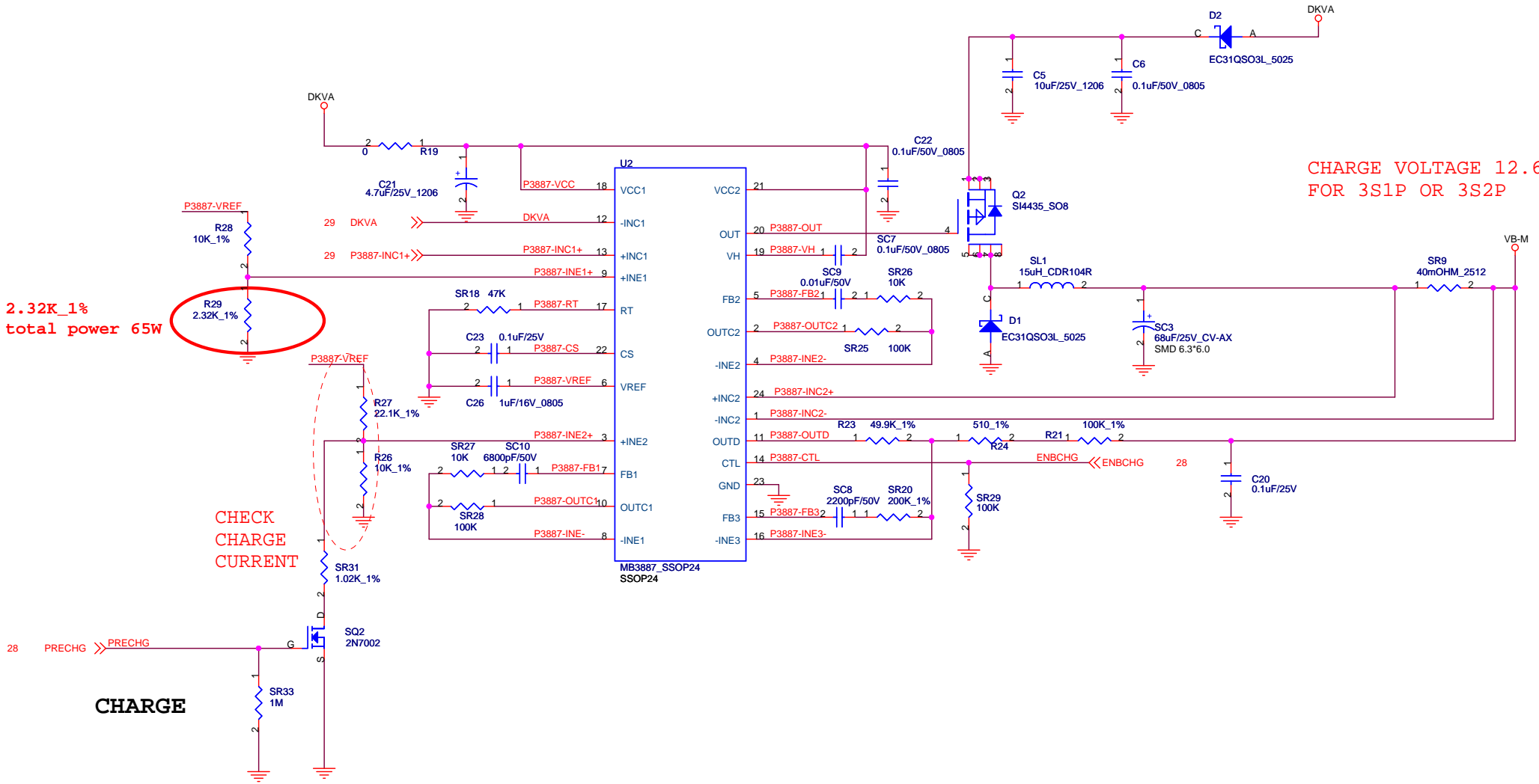
PCIE_1.2V FOR ATI 2A



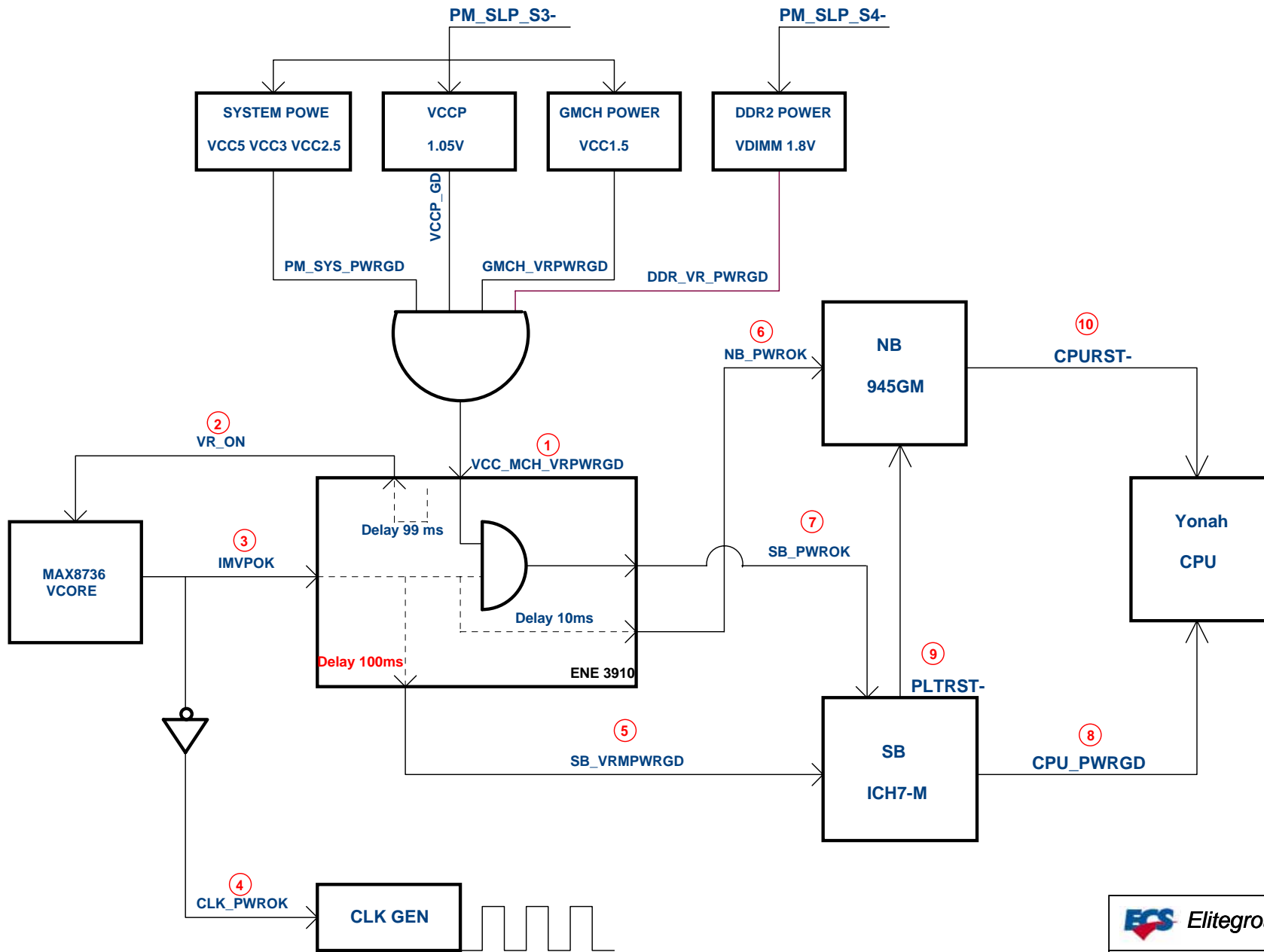
R6 2.32K_1%
for total power 65W

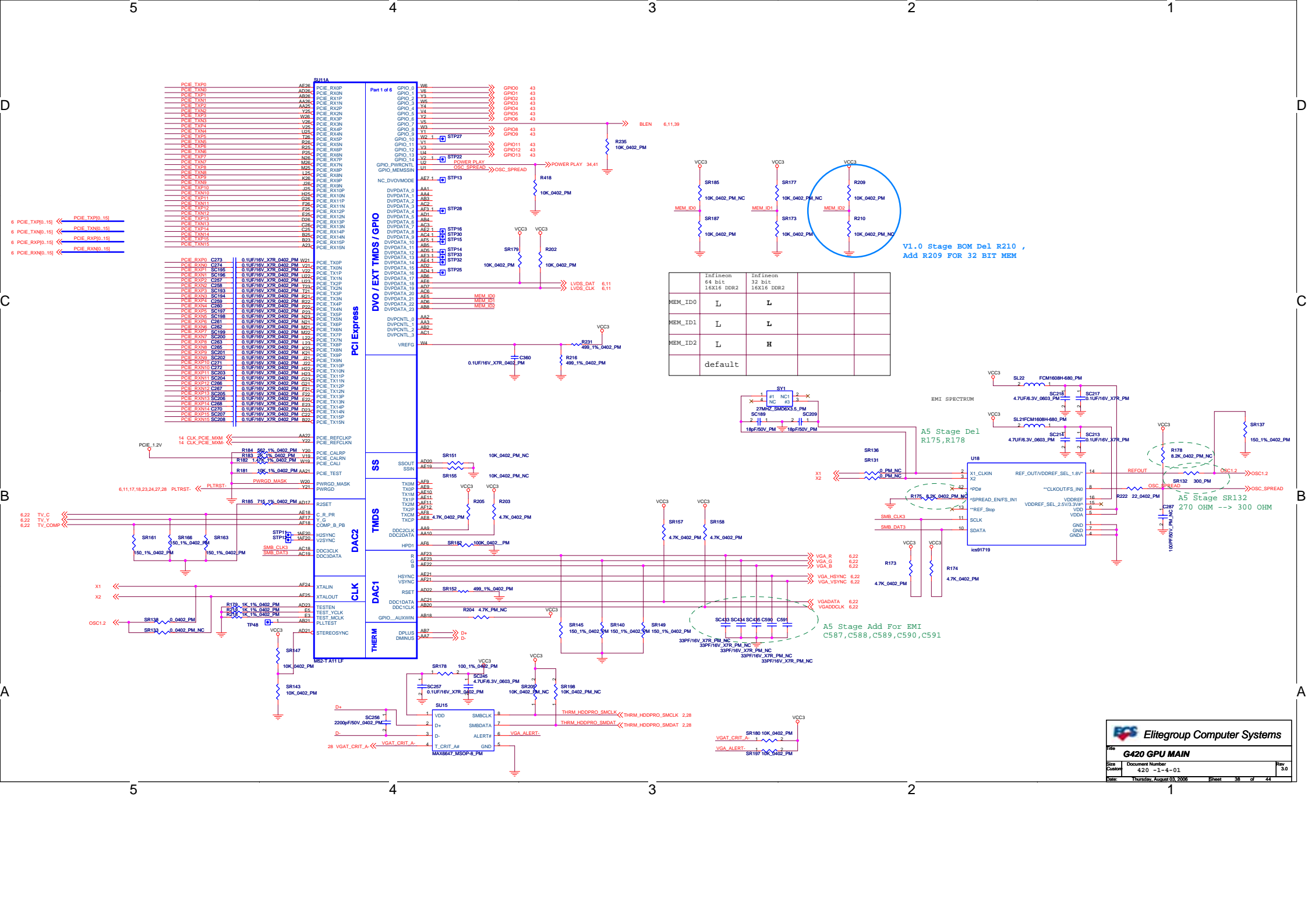
CHECK
CHARGE
CURRENT

CHARGE VOLTAGE 12.6V
FOR 3S1P OR 3S2P



ECS Elitegroup Computer Systems		
Title G420 CHARGER CIRCUIT		
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- 6 PCIe_TXP0_15] << PCIe_TXP0_15]
- 6 PCIe_TXN0_15] << PCIe_TXN0_15]
- 6 PCIe_RXP0_15] << PCIe_RXP0_15]
- 6 PCIe_RXN0_15] << PCIe_RXN0_15]

Part of 6	GPIO_0	GPIO_1	GPIO_2	GPIO_3	GPIO_4	GPIO_5	GPIO_6	GPIO_7	GPIO_8	GPIO_9	GPIO_10	GPIO_11	GPIO_12	GPIO_13	GPIO_14	GPIO_PWCNTN	GPIO_MEMSSIN	NC_DV0VMODE	DVPDATA_0	DVPDATA_1	DVPDATA_2	DVPDATA_3	DVPDATA_4	DVPDATA_5	DVPDATA_6	DVPDATA_7	DVPDATA_8	DVPDATA_9	DVPDATA_10	DVPDATA_11	DVPDATA_12	DVPDATA_13	DVPDATA_14	DVPDATA_15	DVPDATA_16	DVPDATA_17	DVPDATA_18	DVPDATA_19	DVPDATA_20	DVPDATA_21	DVPDATA_22	DVPDATA_23	DVPDATA_24	DVPDATA_25	DVPDATA_26	DVPDATA_27	DVPDATA_28	DVPDATA_29	DVPDATA_30	DVPDATA_31	DVPDATA_32	DVPDATA_33	DVPDATA_34	DVPDATA_35	DVPDATA_36	DVPDATA_37	DVPDATA_38	DVPDATA_39	DVPDATA_40	DVPDATA_41	DVPDATA_42	DVPDATA_43	DVPDATA_44	DVPDATA_45	DVPDATA_46	DVPDATA_47	DVPDATA_48	DVPDATA_49	DVPDATA_50	DVPDATA_51	DVPDATA_52	DVPDATA_53	DVPDATA_54	DVPDATA_55	DVPDATA_56	DVPDATA_57	DVPDATA_58	DVPDATA_59	DVPDATA_60	DVPDATA_61	DVPDATA_62	DVPDATA_63	DVPDATA_64	DVPDATA_65	DVPDATA_66	DVPDATA_67	DVPDATA_68	DVPDATA_69	DVPDATA_70	DVPDATA_71	DVPDATA_72	DVPDATA_73	DVPDATA_74	DVPDATA_75	DVPDATA_76	DVPDATA_77	DVPDATA_78	DVPDATA_79	DVPDATA_80	DVPDATA_81	DVPDATA_82	DVPDATA_83	DVPDATA_84	DVPDATA_85	DVPDATA_86	DVPDATA_87	DVPDATA_88	DVPDATA_89	DVPDATA_90	DVPDATA_91	DVPDATA_92	DVPDATA_93	DVPDATA_94	DVPDATA_95	DVPDATA_96	DVPDATA_97	DVPDATA_98	DVPDATA_99
AE20	AE21	AE22	AE23	AE24	AE25	AE26	AE27	AE28	AE29	AE30	AE31	AE32	AE33	AE34	AE35	AE36	AE37	AE38	AE39	AE40	AE41	AE42	AE43	AE44	AE45	AE46	AE47	AE48	AE49	AE50	AE51	AE52	AE53	AE54	AE55	AE56	AE57	AE58	AE59	AE60	AE61	AE62	AE63	AE64	AE65	AE66	AE67	AE68	AE69	AE70	AE71	AE72	AE73	AE74	AE75	AE76	AE77	AE78	AE79	AE80	AE81	AE82	AE83	AE84	AE85	AE86	AE87	AE88	AE89	AE90	AE91	AE92	AE93	AE94	AE95	AE96	AE97	AE98	AE99	AE100																																						

	Infinion 64 bit 16x16 DDR2	Infinion 32 bit 16x16 DDR2
MEM_ID0	L	L
MEM_ID1	L	L
MEM_ID2	L	H
	default	

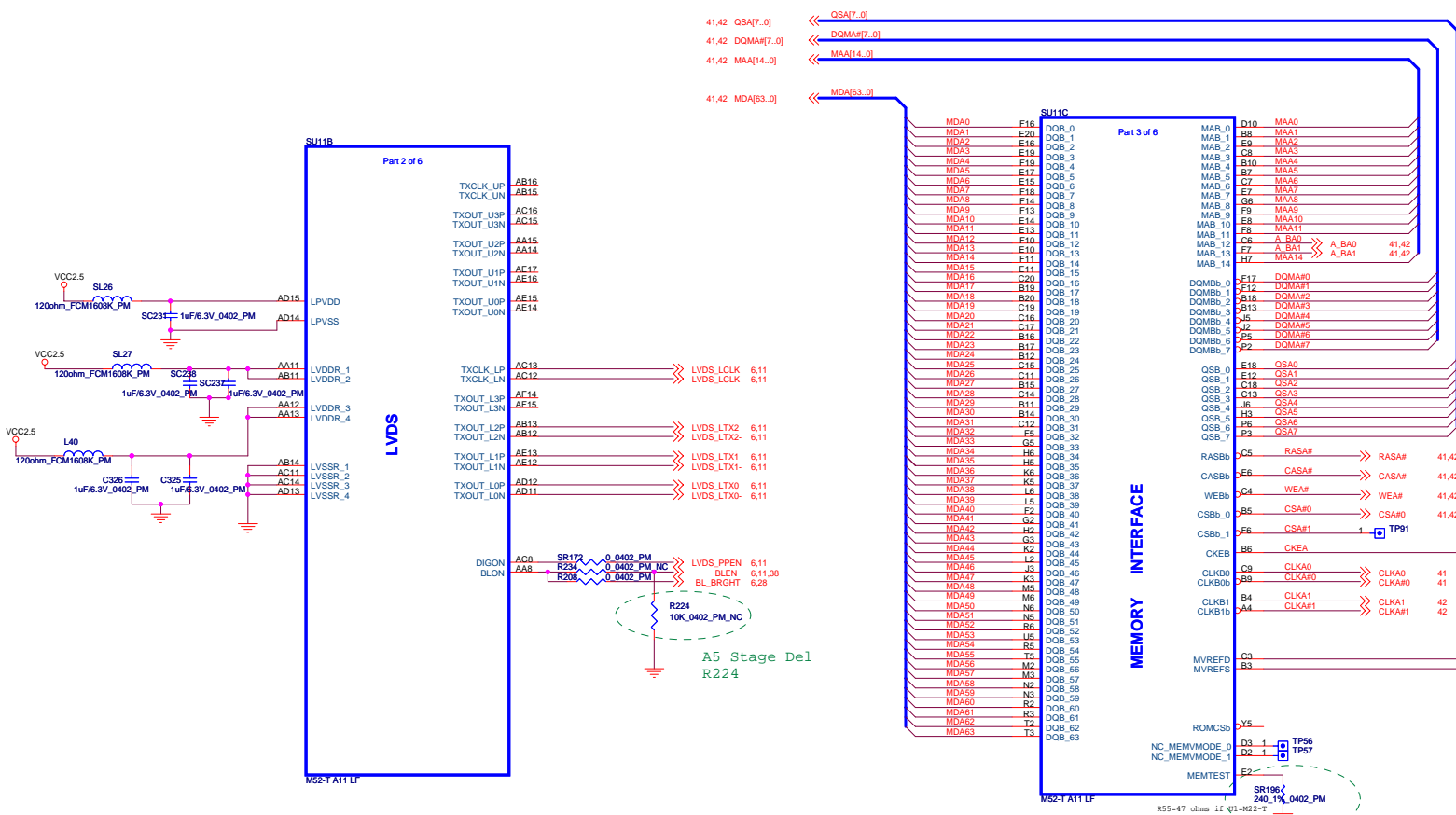
V1.0 Stage BOM Del R210, Add R209 FOR 32 BIT MEM

A5 Stage Add For EMI C587, C588, C589, C590, C591

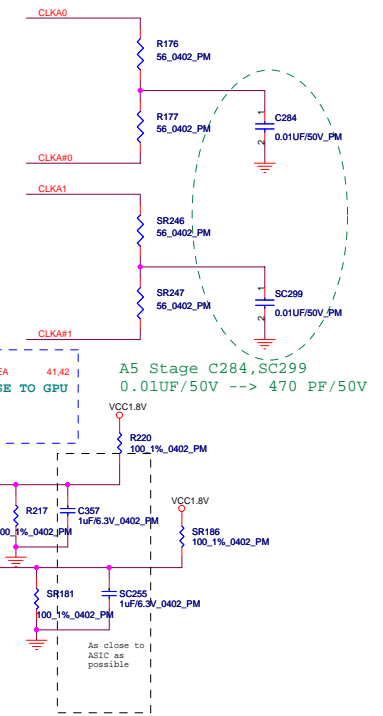
		G420 GPU MAIN	
		Document Number 420 -1-4-01	Rev 3.0
Date: Thursday, August 05, 2006	Sheet 38	of	44

D
C
B
A

D
C
B
A

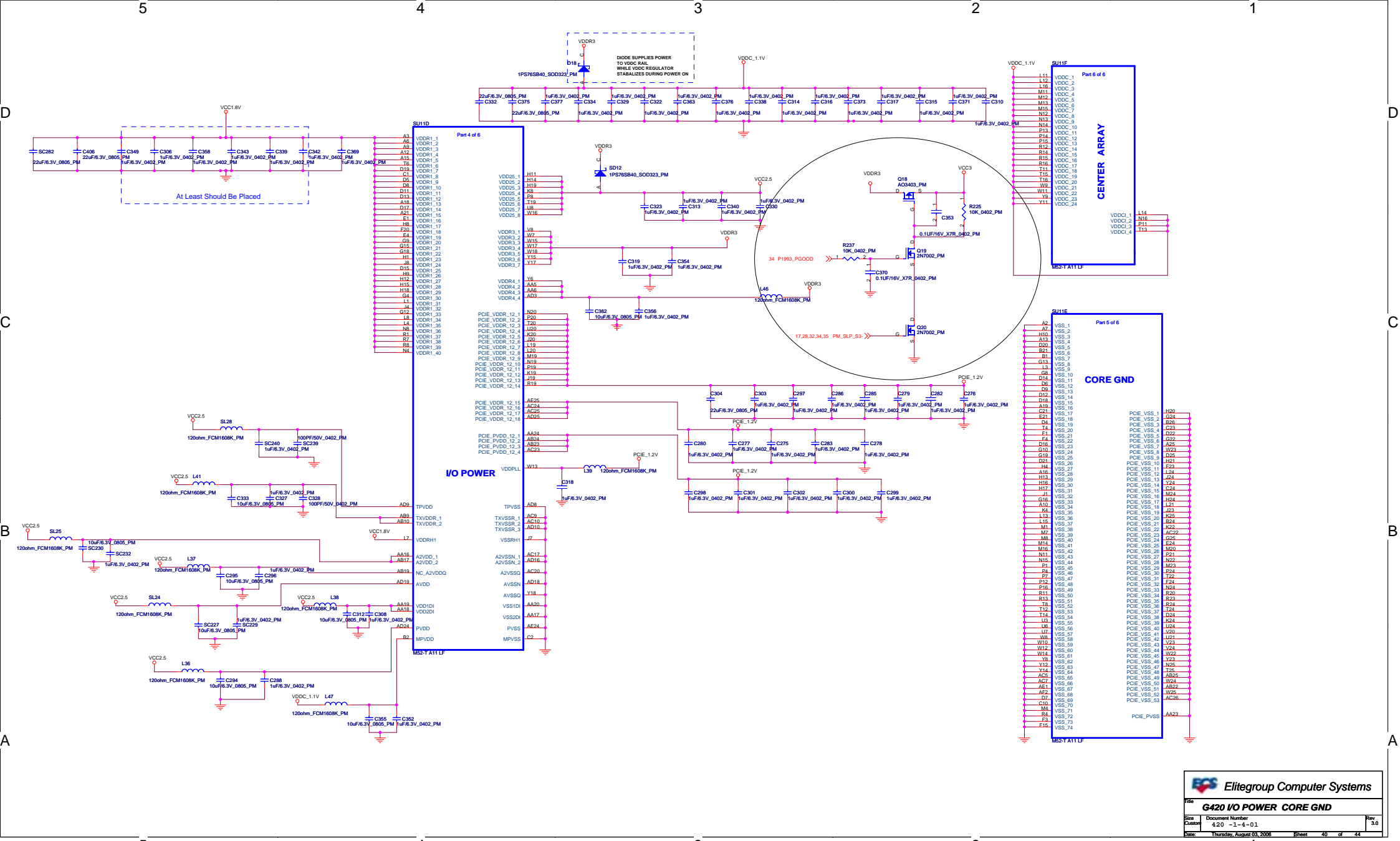


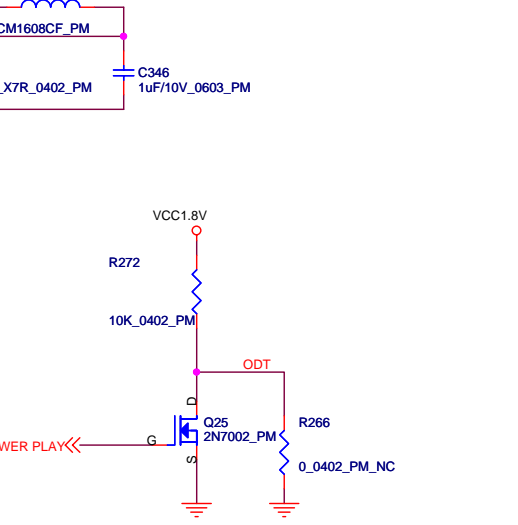
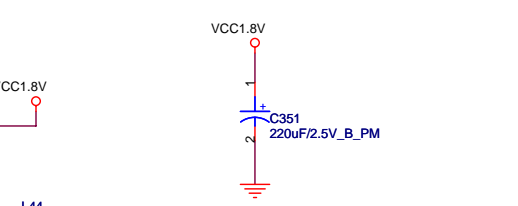
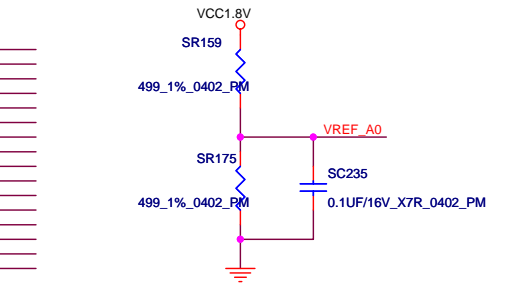
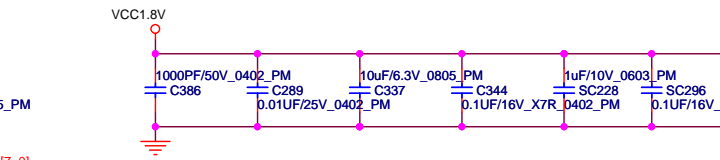
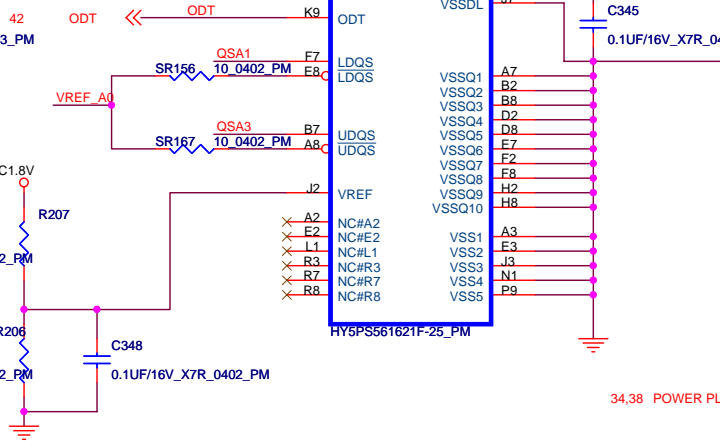
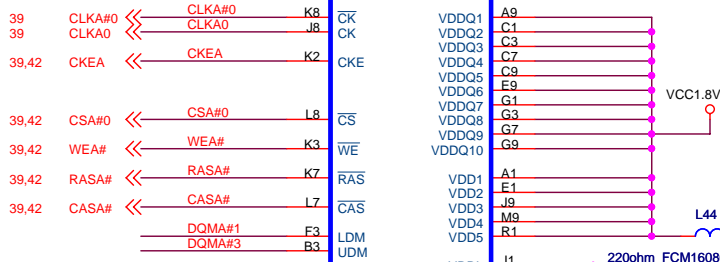
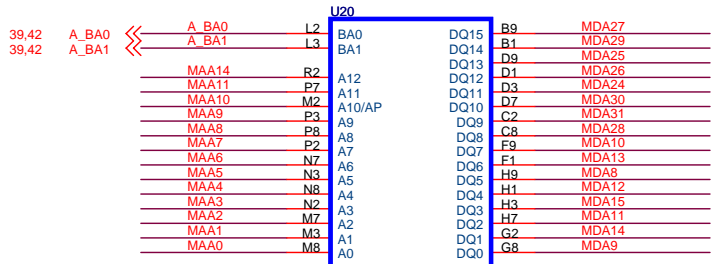
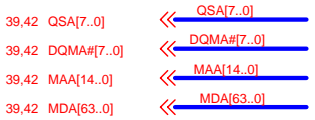
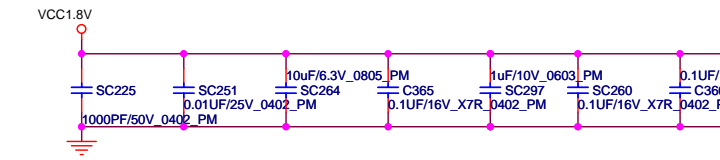
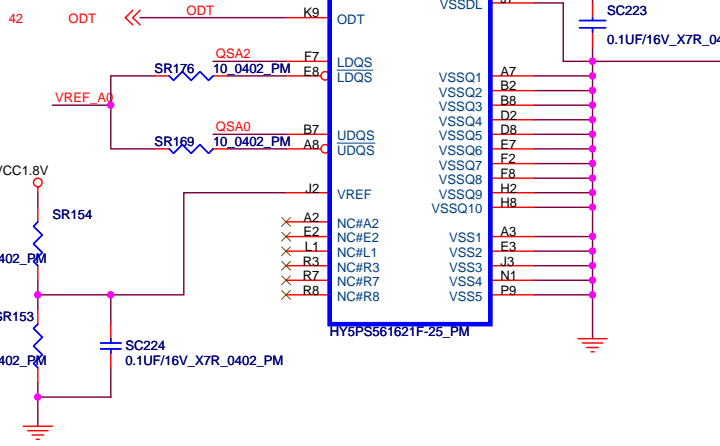
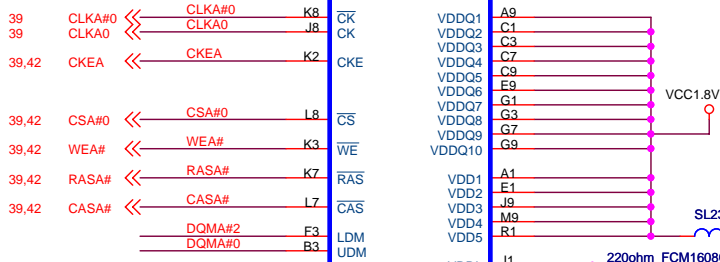
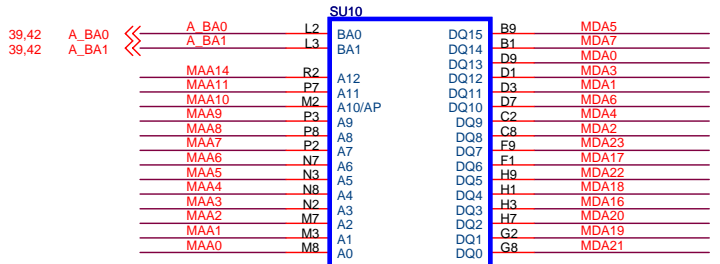
CLOCK termination



MEMORY CHANNEL B

A5 Stage SR196 243 OHM --> 240 OHM



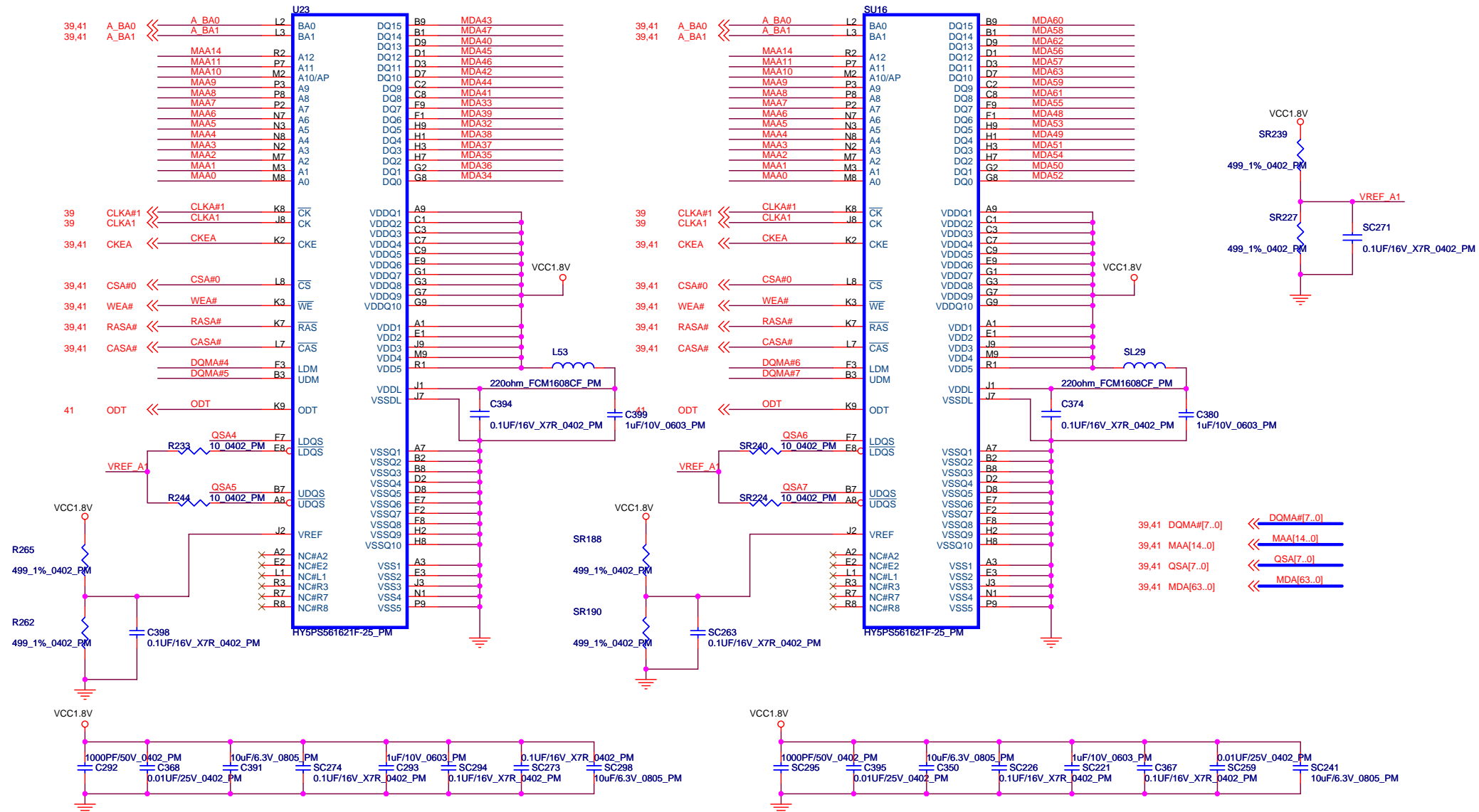


ECS Elitegroup Computer Systems

Title: **G420 DDR2 VRAM 16X16 A**

Size B	Document Number	Rev
420	-1-4-01	3.0

Date: Thursday, August 03, 2006 Sheet 41 of 44



Elitegroup Computer Systems

Title: **G420 DDR2 VRAM 16X16 B**

Size: 420 -1-4-01

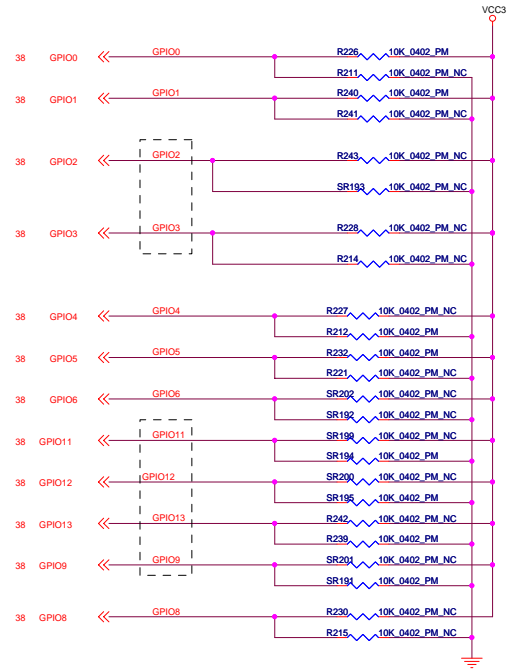
Document Number: 420 -1-4-01

Date: Thursday, August 03, 2006

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Rev: 3.0

OPTION STRAPS



STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing 1.full Tx output swing	
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1.Tx de-emphasis enabled	
	GPIO(3:2)	RSVD	
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible (Debug_Access on M22T is GPIO8)	0
	GPIO5	RSVD	
	GPIO6	RSVD	
Force_Compliance	GPIO8	Force chip to get to compliance state quickly for Tester purposes	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Amel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM 1100 - Serial M25P05 ROM (ST), chip IDis from ROM 1100 - Serial N25F011B ROM (ISS), chip IDis from ROM	
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port device present. 1-No slave VIP port devices reporting presence during reset	No default
	H2VSYNC, V2VSYNC, GENERIC	RSVD	
	VSYNC	RSVD	
	HSYNC	RSVD	
	PCIE_TEST	RSVD	

MULTIFUNC(1:0)	LCDDATA(17:16)	Multi-function device select 00 - single function device 01 - two function device. No AGP in either function 10 - two function device. AGP only in function 0 11 - two function device. AGP in both functions If BUSCFG pin based straps are set to PCI, then AGP will not be enabled in any function.	00
VIP_DEVICE	LCDDATA(20)	Indicates if any slave VIP host devices drove this low during reset. 0 - Slave VIP host port devices present 1 - No slave VIP host port devices reporting presence during reset	0
DWNGRD	LCDDATA(21)	0 - Device remain a workstation grade part. 1 - Part is downgraded to a Normal part	0 (internal pull-down)

420 M/B V.A initial release-05/10/21


420 M/B V.C initial release-06/02/20

P.22 CN2 PIN SWAP

420 M/B V.1.0 initial release-06/04/03

420 M/B V2.0 MODIFY PLEAST RESET PIN BUG

420 M/B V3.0 MODIFY GLAN

		
Title G420 HISTORY		
Size Custom	Document Number 420 -1-4-01	Rev 3.0
Date:	Thursday, August 03, 2006	Sheet 44 of 44