Agenda for the document

- Power well background introduction
- Power well cases causing audio crash
- Private API implementation overview
- The working sequence analysis
- Some logs during test

For Intel Haswell , “power well” in GPU has impact for both Display HD-A controller and codecs. Gfx driver has power well feature enaled but donot think much about audio side. The issue Is if gfx driver disabled power well, audio side would lose power and crash.

This document introduced some background about power well design for haswell hardware, the diagram would give you a overall picture. Also there’s a patchset intend to add private API between i915 and hd-a driver, which fix the power well dependency issue.

David helped a initial patch to add external module patch_hdmi_i915, which built in only DRM_I915 and HDMI_CODEC enabled, This patchset was based on David’s work, thanks David! As codec depends on controller’s power, so we removed the pm callback temporary, bur leave the module model there.

1. Gfx driver would shutdown power well in below cases, audio driver would be damaged as losing power totally without any notification. (There would be more cases not covered, welcome more comments here.i can verify the patchset under more cases)

- Only eDP port active
- HDMI monitor hot plug
- System suspend

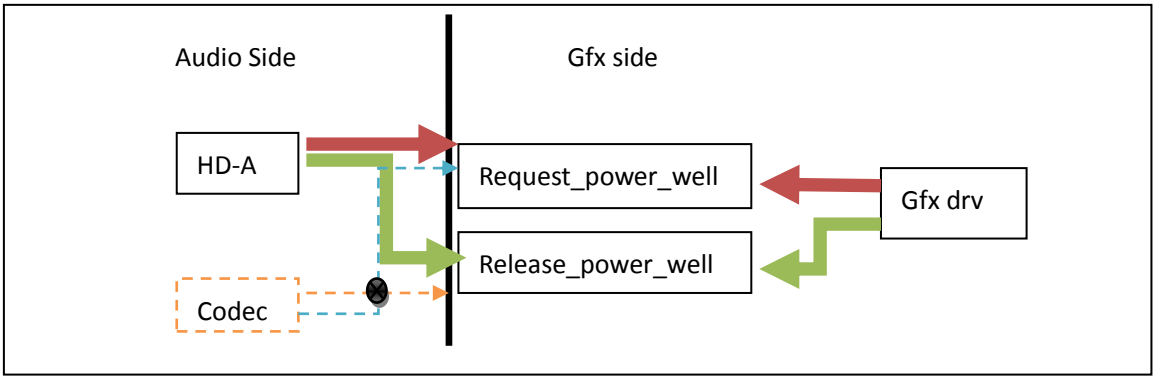
Also there’re some calling from i915 to disable power well from time to time, this patchset would reject those operations if audio using power well, but it will record i915 driver’s request and shut down power if audio release it.

2. Basiclly, gfx driver provides such interface for display audio in Alsa driver side.

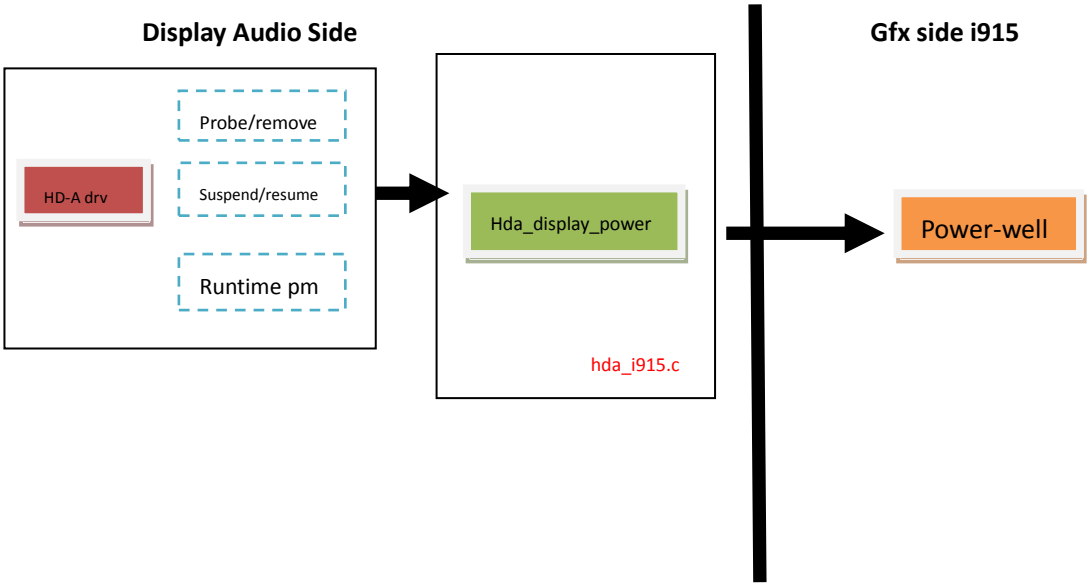
Note

Red: power well request operation

Green: power well release operation



3. The power well feature implementation for display audio:



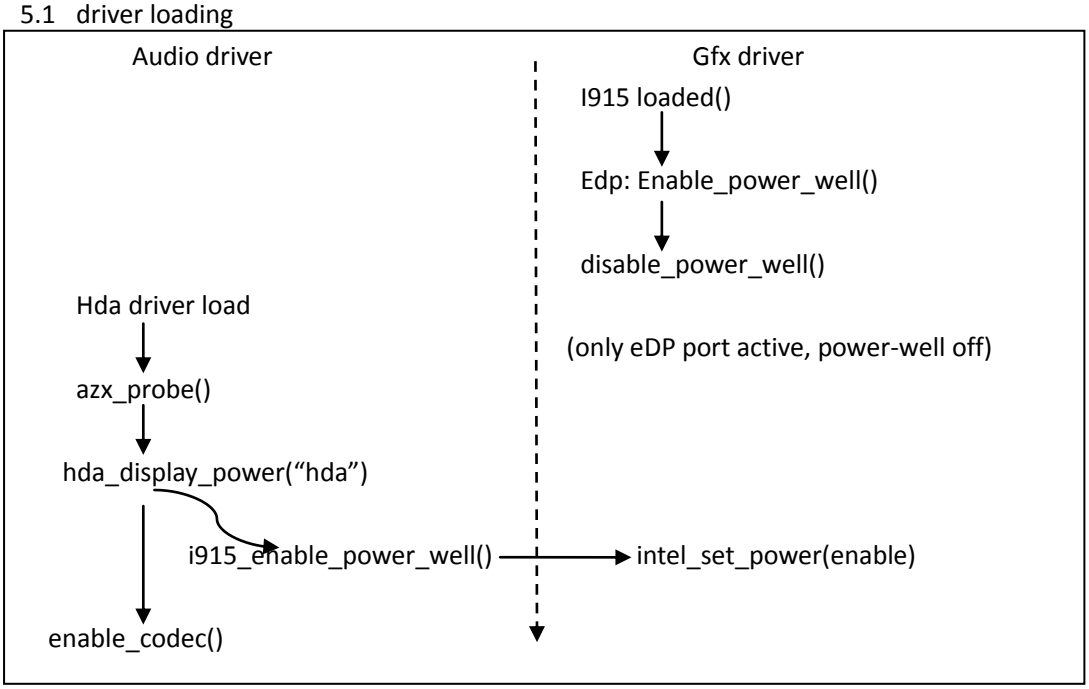
Note:

1) Hda_i915 is the external module, depends on i915 and snd_hda_intel, only built in when both modules enabled.
2) Hda_display_power depends on hda_i915, it's null if hdmi_i915 not built in.

4. Working sequence:

(Only eDP port case for HSW ult board)

5.1 driver loading

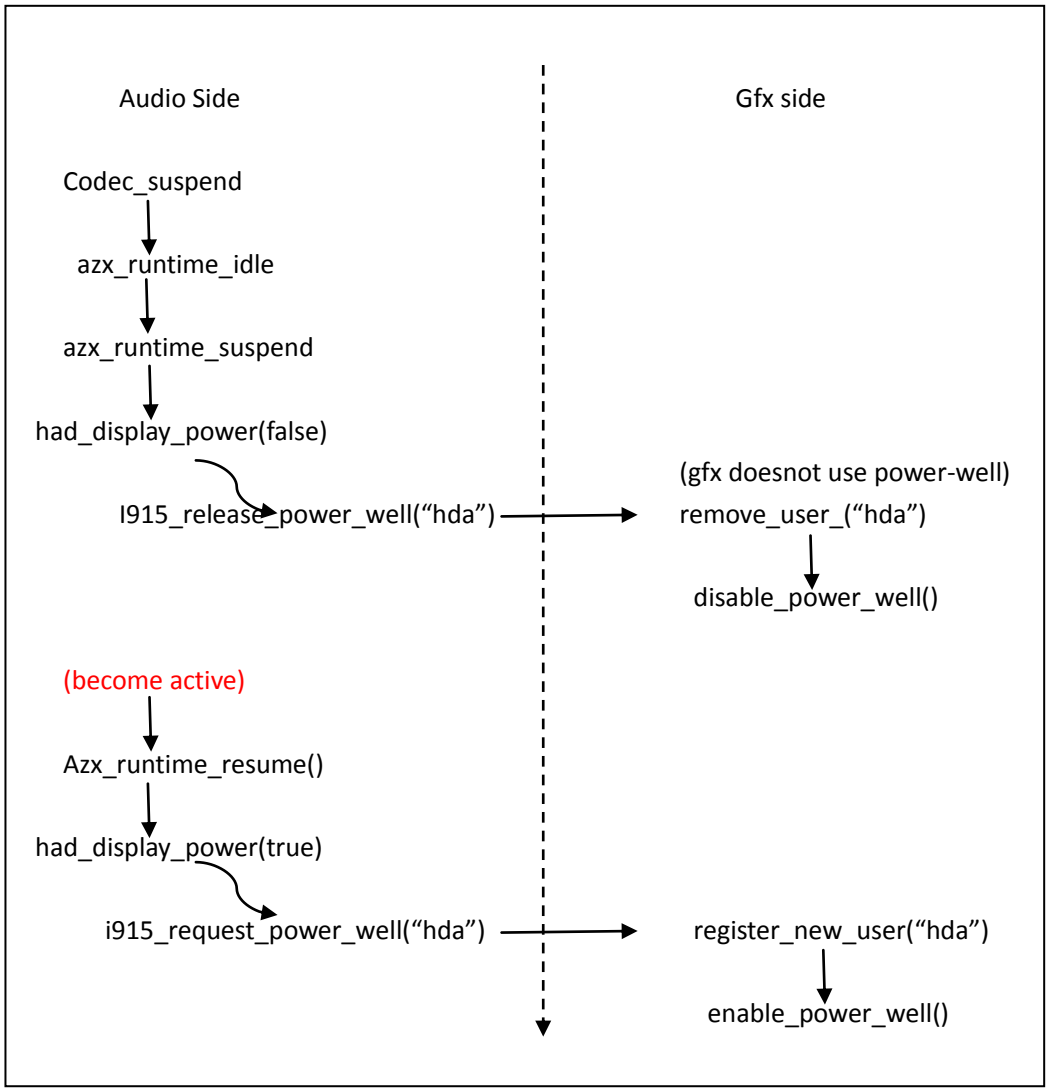


4.2 power save mode:

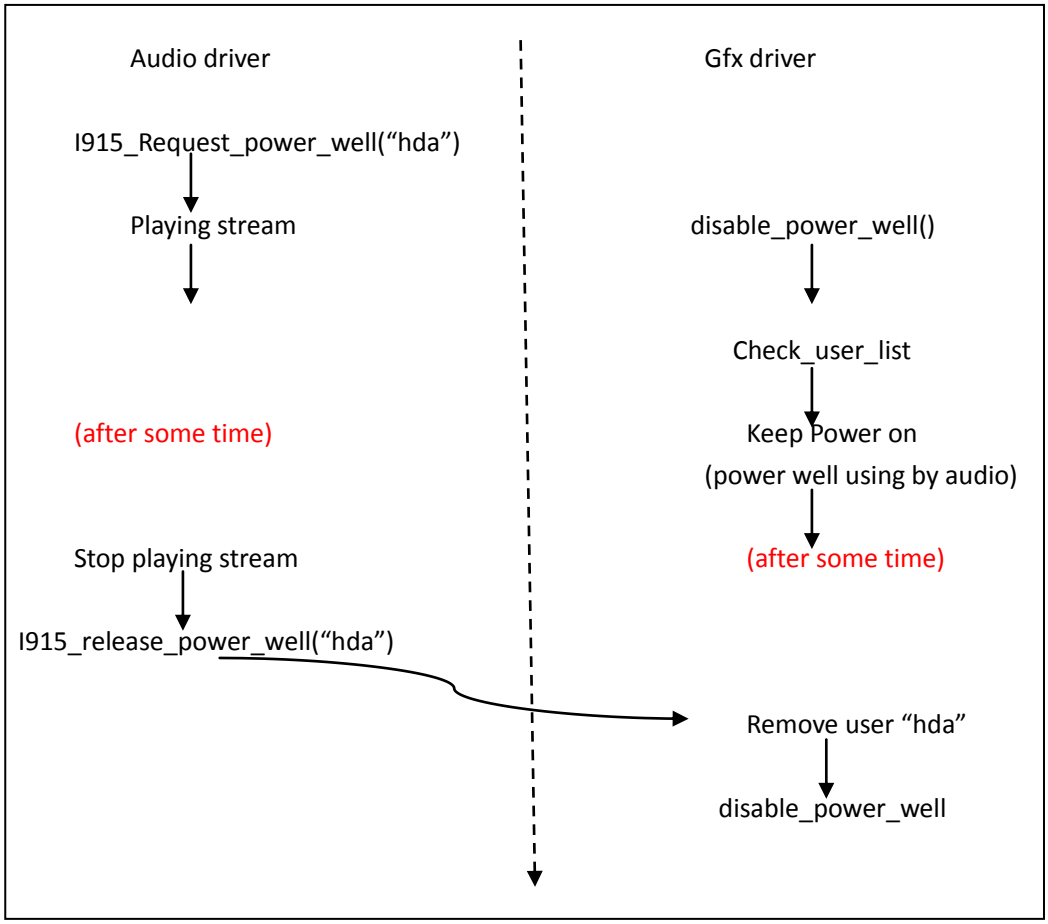
enable power_save for codec by:

echo 5 > /sys/module/snd_hda_intel/parameters/power_save

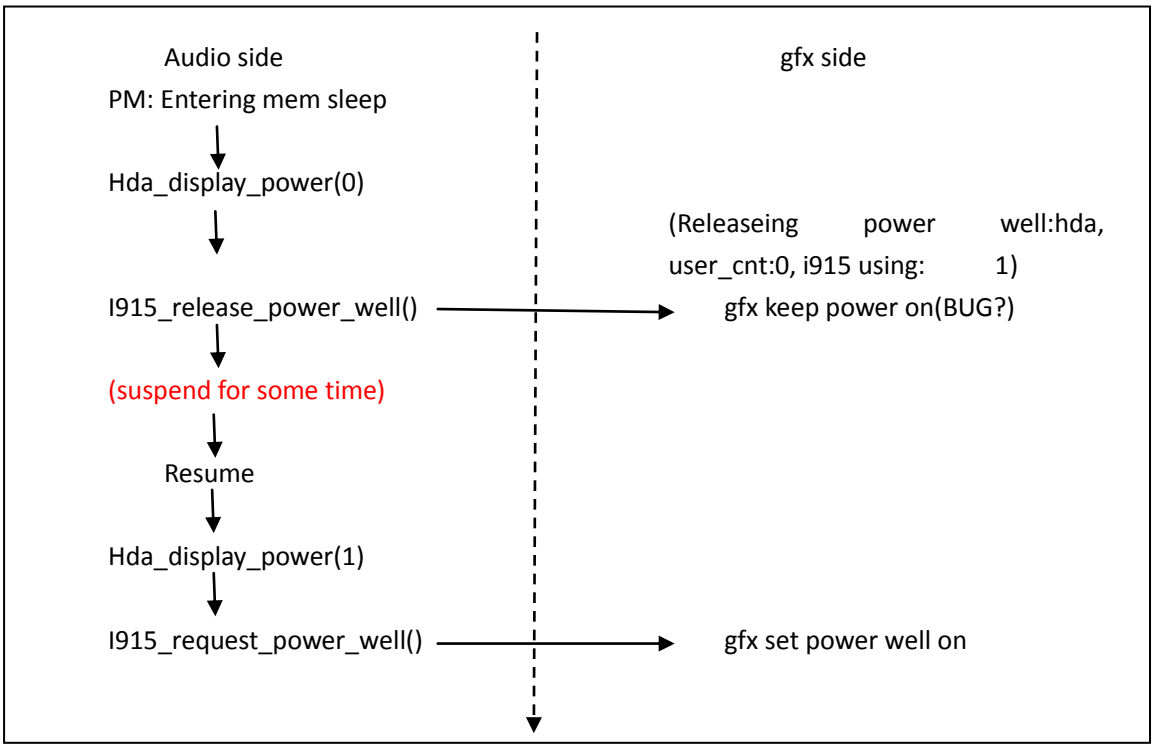
power-save for hd-a controller is enabled by default. Codec will enter suspend mode if it's inactive in 5 seconds. Then HD-A controller will enter suspend too.



4.3 gfx disable power-well



5.4 echo mem > /sys/power/state



5. Logs: (red color for key message)

6.1 hd-a controller initialize

[7.980427] [drm] Initialized i915 1.6.0 20080730 for 0000:00:02.0 on minor 0

[7.996140] init: plymouth-splash main process (1187) terminated with status 1

[8.000242] [drm:intel_crtc_set_config], [CRTC:3] [FB:12] #connectors=1 (x y) (0 0)

[8.000246] [drm:intel_modeset_stage_output_state], [CONNECTOR:10:eDP-1] to [CRTC:3]

[8.045450] HDA display power 1

[8.045456] [drm:i915_request_power_well], request power well for hda

[8.045460] [drm:set_power_well], Enabling power well

[8.045462] [drm:i915_request_power_well], hda set power well on

[8.045643] snd_hda_intel 0000:00:03.0: irq 63 for MSI/MSI-X

[8.046221] [drm:intel_panel_actually_set_backlight], set backlight PWM = 0

[8.046226] [drm:ironlake_edp_backlight_off],

5.2 runtime power save

[247.509629] Codec enter suspend →codec suspend after 5 seconds free

[247.533680] Azx runtime idle

[247.533689] Azx runtime suspend → controller suspend too

[247.533696] HDA display power 0 →release power well

[247.533701] [drm:i915_release_power_well], release power well from hda

[247.533708] [drm:i915_release_power_well], Releaseing power well:hda, user_cnt:0, i915 using:0 →power well shutdown as gfx doesnot use

[247.533714] [drm:set_power_well], Requesting to disable the power well

[262.181277] Azx runtime resume →controller resume

[262.181287] HDA display power 1

[262.181292] [drm:i915_request_power_well], request power well for hda

[262.181301] [drm:set_power_well], Enabling power well →*enable power well as "hda" is first user*

[262.181305] [drm:i915_request_power_well], hda set power well on

[262.183683] Codec start resume

[262.184299] hda_codec: invalid CONNECT_LIST verb 3[1]:0

[267.199811] Codec enter suspend

[293.880274] Codec start resume

[308.837280] Codec enter suspend

[308.861329] Azx runtime idle

[308.861339] Azx runtime suspend

[308.861347] HDA display power 0

[308.861353] [drm:i915_release_power_well], release power well from hda

[308.861360] [drm:i915_release_power_well], Releaseing power well:hda, user_cnt:0, i915 using:0

[308.861366] [drm:set_power_well], Requesting to disable the power well

[424.272995] Azx runtime resume

[424.273004] HDA display power 1

[424.273010] [drm:i915_request_power_well], request power well for hda

[424.273019] [drm:set_power_well], Enabling power well

5.3 gfx disable power well but audio using

[228.732486] [drm:intel_dp_compute_config], DP link bw 0a lane count 2 clock 270000 bpp 24

[228.732486] [drm:intel_dp_compute_config], DP link bw required 333072 available 432000

[228.732487] [drm:intel_dp_compute_config], clamping display bpc (was 24) to eDP (24)

[228.732488] [drm:intel_modeset_pipe_config], [CRTC:3]

[228.732489] [drm:intel_modeset_pipe_config], plane bpp: 24, pipe bpp: 24, dithering: 0

[228.732490] [drm:intel_set_power_well], Display audio power well busy using now

[228.732493] [drm:haswell_crtc_mode_set], Mode for pipe A:

[228.732495] [drm:drm_mode_debug_printmodeline], Modeline 0:"1920x1080" 60 138780 1920 1966 1996 20

80 1080 1082 1086 1112 0x48 0xa

[228.732506] [drm:ironlake_update_plane], Writing base 00074000 00000000 0 0 7680

[228.795958] [drm:ironlake_wait_for_vblank], vblank wait timed out

[228.795985] [drm:intel_crtc_mode_set], [ENCODER:9:TMDS-9] set [MODE:0:1920x1080]